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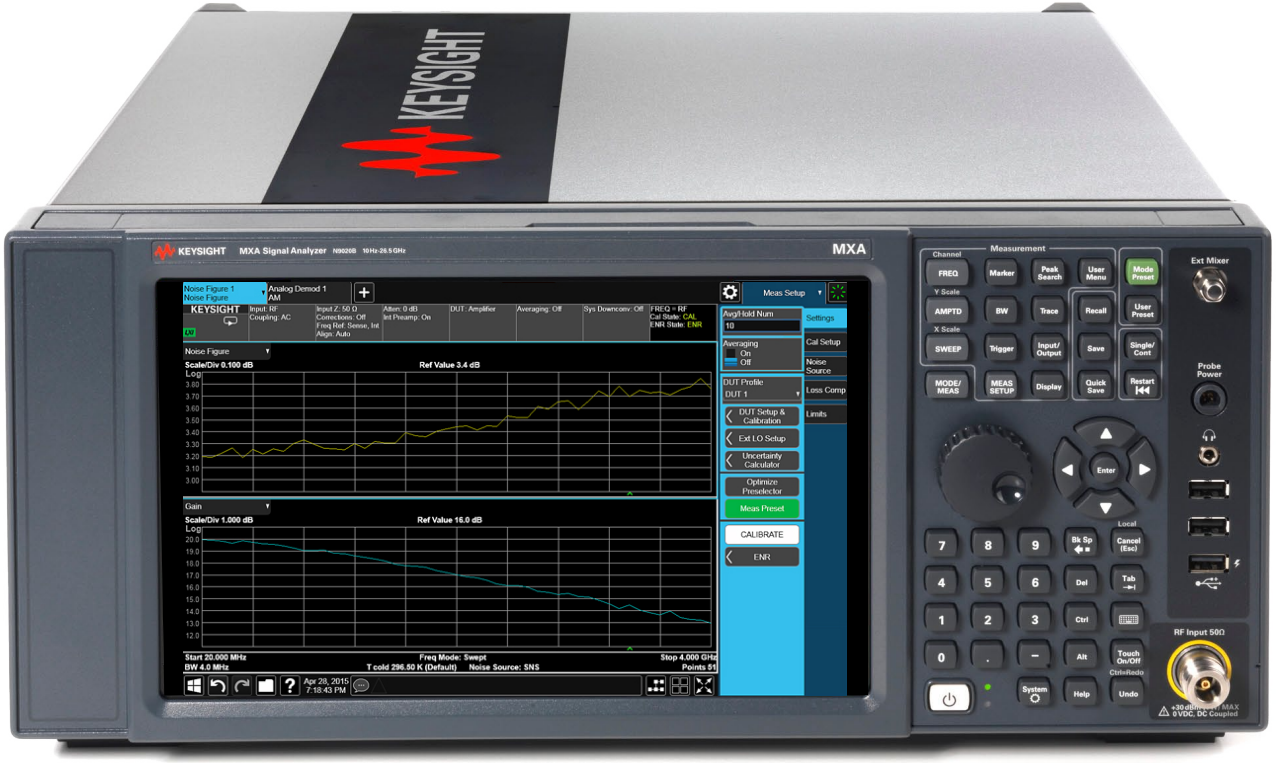
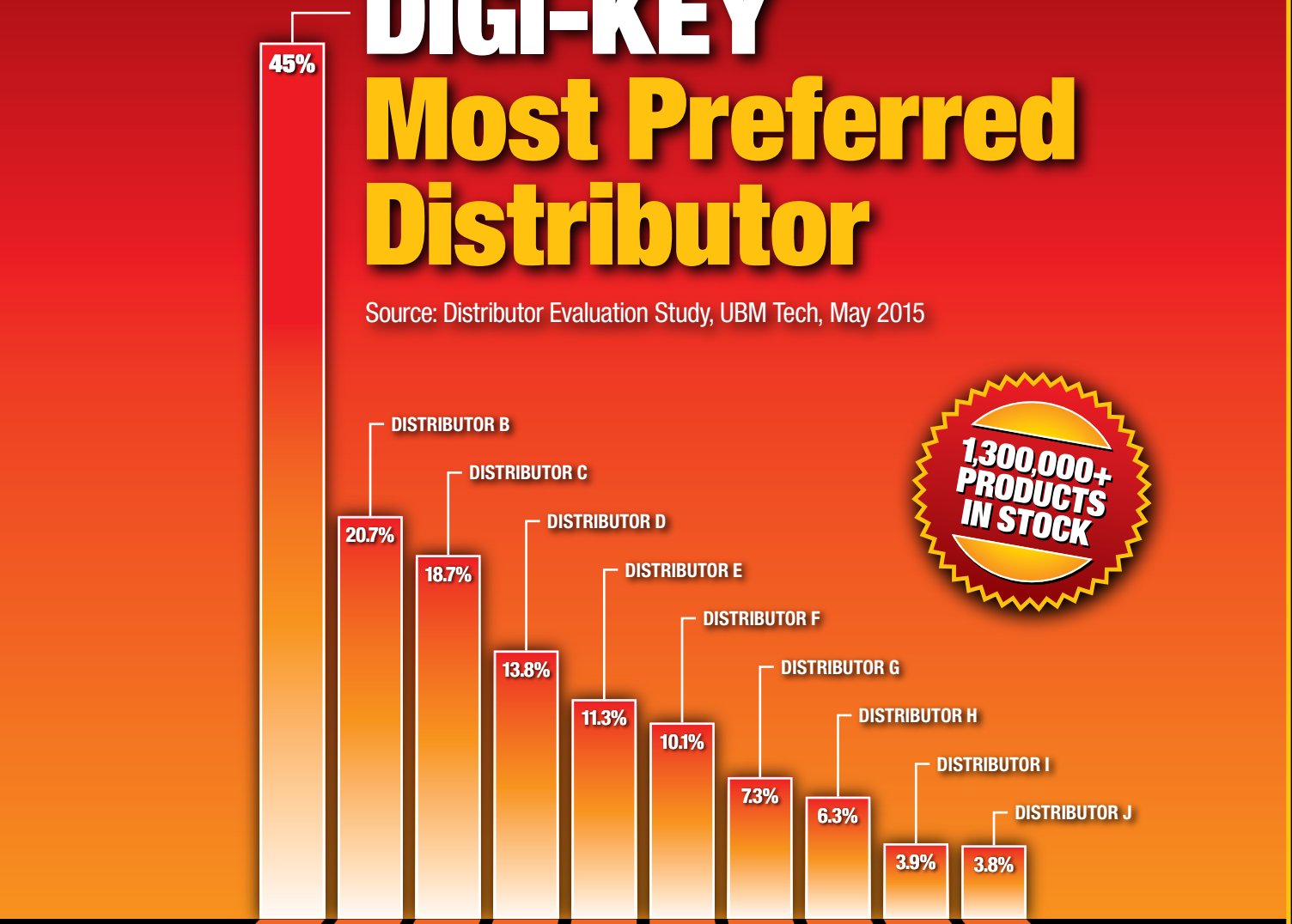
Keysight Technologies X-Series Measurement Application

Improve your noise figure measurements.



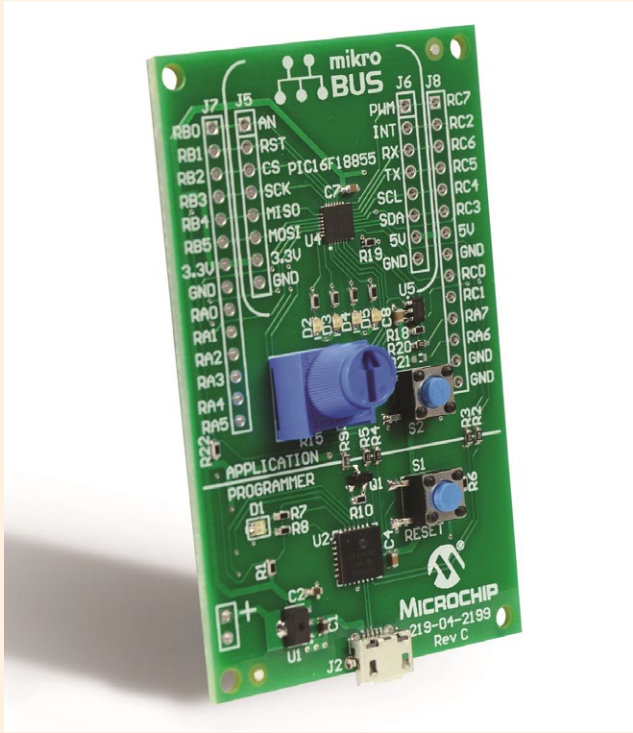
DIGI-KEY
Most Preferred Distributor

Source: Distributor Evaluation Study, UBM Tech, May 2015



COVER

Microchip opts for cloud-based IDE to attract PIC 'newbies'



Microchip Technology recently gave away thousands of these MPLAB Xpress Evaluation Boards as part of its launch of a cloud-based design environment for PIC microcontrollers. The programme is, in part, intended to introduce the architecture to non-PIC aficionados from hobbyist through to professional, and the software promises that you can do real development work, without even the need to register – more on page 17 of this issue.

FEATUREARTICLES

ONLINE THIS MONTH

Toolbox for MATLAB enables faster and more robust WLAN design

Implementing an IoT end-point SoC platform with minimal engineering resources

EDN's columns

SAFE AND SECURE

Attending the embedded world exhibition in February, I heard – you will not be surprised to learn – many presentations on silicon, software and systems for the coming era of connected devices. Yes; the Internet of Things. And as part of that, much content on providing the necessary security aspects. At least, as the IoT bandwagon rolls on, the industry recognises that there is a security issue; and it is energetically engaged in providing all of the component parts needed to embed security. Microcontrollers for connected-device roles now routinely come with on-board cryptography engines; secure operating systems migrate from the big-systems world to the coin-cell-powered space; IoT 'back-office' infrastructure offerings boast their levels of protection against intrusion. All the components you might need are already out there.

Why, therefore, am I not entirely convinced? It is the very complexity of providing an end-to-end secure context for the IoT data traffic: and the need for it to be, in that favourite term of the marketer, "seamless". IoT systems will present – we will all have to take on board the jargon – a very large attack surface. Every aspect of a system will have to have security embedded from the outset, will have to work together correctly, will not contain code of doubtful provenance re-used from older projects – the list goes on.

The environment has also changed. The rule-of-thumb metric for assessing security was once; a system is safe if the effort to attack it significantly outweighs the gains the attacker might make. That is no longer the case. There is a world of hackers that will delight in applying virtually unlimited effort to penetrating the barriers around any product that claims to be secure, for no more gain than the kudos of having done so. And the "pro" hackers have not gone away.

The risks are high. A handful of high-profile cases of data loss could damage perceptions of the entire connected-device project. Even without that happening, on the consumer side the buying public will have to be convinced that the benefits to be had from connectivity (connected-ness?) are worth the risks. I heard one industry executive attending embedded world express it like this (he named a brand of connected domestic heating controller, and an Internet services provider, which I should perhaps not quote), "Am I going to install a device that uploads data to the net, and stores it who-knows-where – even if the provider assures me that data is safe – that has embedded in it, information about when I'm at home and when my house is unattended? Just so I can turn up the heating from my phone? I don't think so." Insiders are often the hardest to sell to, but the concern is completely understandable.

The range of product offerings for IoT design is also coming to reflect the fact that this is a different context. We are all familiar with the regular update cycle that it takes to maintain protection against malware on our desktop and mobile computing platforms. An embedded operating system may be tiny compared, say, to Windows. But applying patches to it will be a challenging problem: the device will have to be designed with sufficient resources to support an update cycle (enough memory to store new and fall-back versions, for example) plus routines sufficiently robust to withstand attack before, during and after an update. And patches will be needed in products that are – as we are constantly told – intended to operate unattended for years or even decades. The intention is that IoT devices proliferate in millions; how to ensure that essential updates propagate to every active unit?

More insidious than the vulnerability of the IoT product itself, is the potential for it to act as a gateway. It is, after all, 'connected', and in its long expected life, it may come to be connected in ways not envisaged by the original design team.

It may be an unduly pessimistic point of view, but considering the multiple challenges of making these new product concepts secure, and taking into account the fact that even with the best intentions, engineering tends to learn and be shaped by the occasional failure – we should be prepared for some disasters. If the PC and commercial software experience is any sort of guide, we should also be prepared for future in which the security task is never finished. Devices with a selling price of a handful of euros, pounds or dollars, that have a maintenance burden lasting decades: that is the reality of what we are signing up to.

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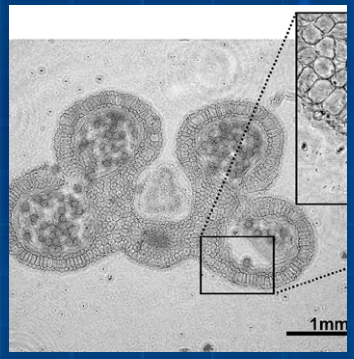
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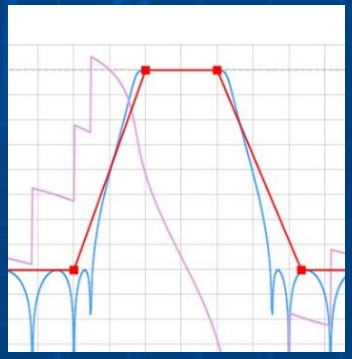
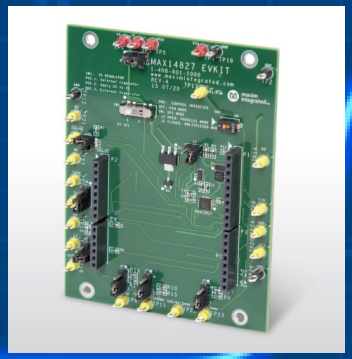



Curiosity
Development Board


MB85RQ4ML


u-blox


MAX14827 EVKIT

Raspberry Pi 3 steps up performance, adds connectivity

The Raspberry Pi Foundation, with distributors RS Components (Electrocomponents) and Farnell element14 have introduced the latest version of the single-board computer; it has a 50% increase in processing power relative to Raspberry Pi 2; and adds on-board wireless connectivity for WiFi and Bluetooth LE.

All of the updates have been achieved while maintaining the original price point of $35. The processor upgrade is to a Quad-core Broadcom BCM2837 64bit ARMv8 processor (running an ARMv7 operating system) at [up to] 1.20 GHz, a significant increase from 900 MHz available with the Raspberry Pi 2. The Broadcom chip uses the Cortex-A53 core.

Eben Upton, CEO of Raspberry Pi Trading (which is the licensing body controlling Raspberry Pi) and originator of the Raspberry Pi Foundation, said that the latest version continues the Foundations's charitable objectives of raising enthusiasm for computer science and engineering among the young, while the availability of on-board Bluetooth LE (and WiFi) firmly positions it as an IoT hub.

Referring to the range of spin-off products that has arisen for embedded computing use, the organisation is, "heading towards Compute Module 3", for release at a later time. In the context of its educational role, Upton says of the Pi 3, "It crosses the line from [possibly being considered as] a toy, to being a full PC... it was never intended to be just a 'worthy' platform."

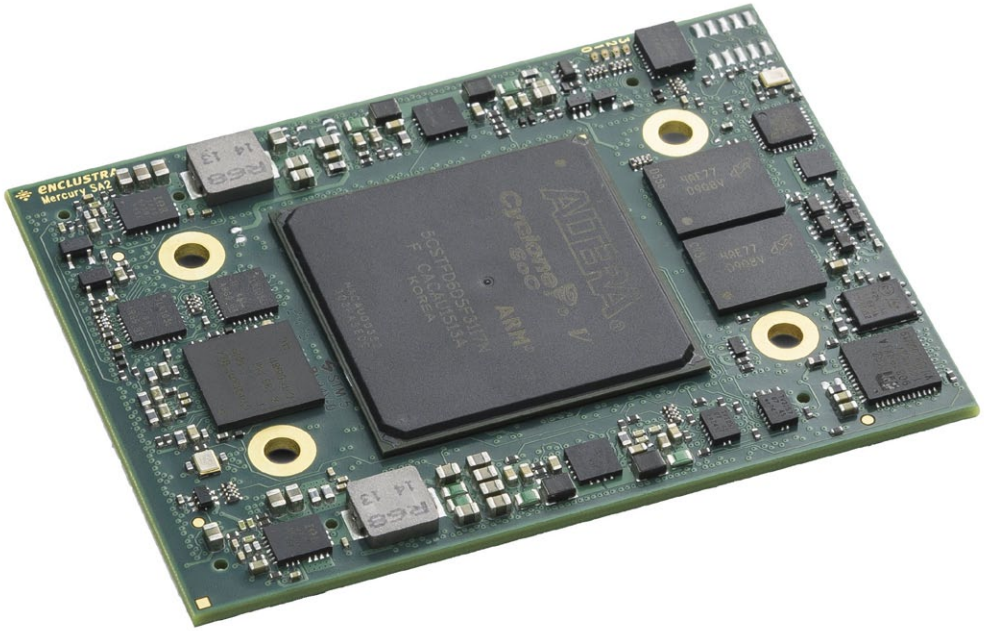
For element14, a spokesman commented on the Raspberry Pi "customisation" offering that was introduced four months previously; the distributor has seen around 300 'opportunities' of which several are approaching realisation. Most projects so far have involved relatively minor changes to the basic platform, around configuring interfaces and peripherals, and cost-reduction. Batch sizes for possible variants start at 5000 units, upwards.

The added on-board connectivity of the model 3 is cited as the largest single gain for embedded users. element14 is adding to its offering of associated products, to include a PiFace interface board, a starter kit (for IoT-class projects) that has been designed with EnOcean and that will use the IBM Bluemix cloud service; an uprated, 2.5A power supply that will power the Pi and any additional boards from a single source; a new moulded case; and a 16 GB NOOBS (New Out Of the Box Software) memory card.

RS Components adds the detail that the connectivity comes from a BCM43438 combo device, which provides 802.11b/g/n wireless LAN, Bluetooth Classic and Bluetooth Low Energy. The main SoC BCM2837 integrates a dual-core VideoCore IV multimedia coprocessor, which provides; 1.2G pixels/sec of fill rate, 1.8 Gtexel/sec of texturing rate; 29 GFLOPs of shader compute throughput; OpenGL ES 1.1/2.0 support; 1080p60 hardware video decoding; 1080p30 hardware video encoding; and a hardware image sensor pipeline. This, Upton comments, represents a small increment of GPU power over the version 2, while the overall CPU performance (over a mixed, general purpose instruction benchmark) is 10x that of the original Pi and 50% up on the Pi 2.

Complete article, here

ARM+FPGA: module hosts Altera Cyclone SoC, offers high I/O count



Enclustra's (Zurich, Switzerland) Mercury+ SA2 is an Altera Cyclone V SoC-based module with over 250 I/Os; the Altera chip gives it a high-performance processor system and many standard interfaces: it is equipped to handle even the most demanding of applications.

The module combines an ARM dual-core Cortex A9 processor with a 28 nm FPGA fabric, all in a package measuring just 74 x 54 mm. The module's 258 user I/Os, 2 GByte DDR3L SDRAM and 64 MByte quad SPI flash combine to form a high-performance processing unit. Multiple interfacing options are also available: 9 MGTs with a data transfer rate of up to 6 Gbps, PCIe Gen1/Gen2 x4, Gigabit Ethernet, dual Fast Ethernet, USB 3.0 and USB 2.0. The module is available in both commercial and industrial temperature range, and needs just a single 5-15 V supply for operation.

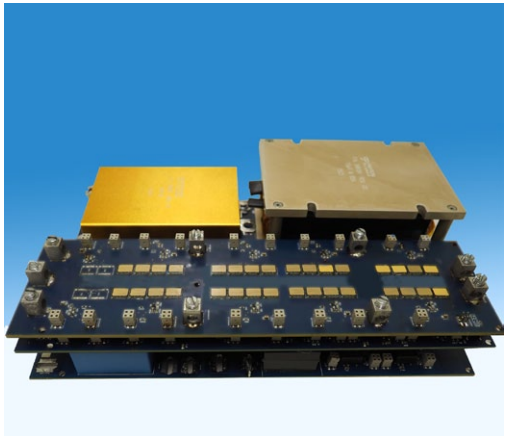
Enclustra also offers a comprehensive ecosystem for the SA2, offering all required hardware, software and support materials. The Mercury+ PE1 base board is a complete development platform for the SA2; detailed documentation and reference designs are available, in addition to the user manual, schema, a 3D-model, PCB footprint and differential I/O length tables.

Complete article, here

Electric-vehicle charger packs 2.6 kW/l, >97% efficiency, with GaN switches

Automotive electronics company Hella, in collaboration with gallium nitride semiconductor maker GaN Systems and charging technology researchers at Kettering University's Advanced Power Electronics Lab (Flint, Michigan, USA), have developed a Level-2 electric vehicle (EV) charger prototype with efficiencies exceeding 97% at an "unprecedented" 2.6 kW/l power density.

Prior to this achievement, Level-2 EV chargers – according to the collaborators – reached maximum efficiencies of 94%. Using GaN Systems' 60A, 650 V GS66516T switches in a two-stage architecture, the Kettering University research team, led by Associate Professor of Electrical Engineering, Dr. Kevin Bai, were able to increase the wall-to-battery efficiency to more than 3% greater



than previously obtained.
Dr. Bai and his team are known for collaborating with companies to help advance their charging technology. Commenting on the importance of this development, Dr. Bai said, “The switching performance we observed with the GaN Systems’ parts was marvellous. Using these devices our power electronics exhibited a power density greater than 2.6 kW/l. This is a significant milestone with important implications for charging electric vehicles, among other charging applications.” Dr. Bai characterised this development as a ‘game changer’ for the EV charging industry.

Complete article, here

Free tools to develop Linux on STM32 MCUs

STMicroelectronics has extended its “design free” tool support to both Linux and Windows platforms, for microcontrollers in the STM32 architecture. Until now, however, (says ST) most development tools for embedded computing have been available only for Windows.
The STM32CubeMX configurator and initialisation tool and the System Workbench for STM32, an Integrated Development Environment (IDE) created by French company Ac6 Tools, supported by the openSTM32.org community, and available at www.st.com/sw-4stm32, are now both available to run on Linux OS.

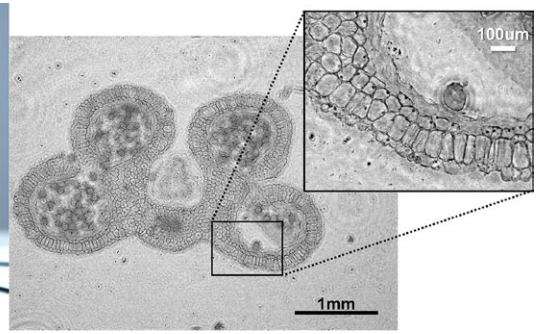
Develop free of charge
under Linux for STM32 MCUs

ST’s latest move means Linux users can now start their own embedded projects on STM32 devices, free of charge, without leaving their favourite desktop environment. Users, ST adds, can now benefit from free software for configuring microcontrollers and developing and debugging code, together with manufacturer-supported low-cost evaluation boards, allowing greater focus on product development. Tools installation is very easy and fast, which contrasts with established practice in the Linux world, where users often have to create or adapt their own tools with minimal support.
System Workbench for STM32 supports the ST-LINK/V2 debugging tool under Linux through an adapted version of the OpenOCD (OpenOCD: Open On-Chip Debug, a free and open project to develop software debug for ARM-based embedded systems, designed to run directly on-chip) community project. Each of these tools can be used in conjunction with ST’s low-cost development hardware including STM32 Nucleo boards, Discovery kits, and Evaluation boards, as well as microcontroller firmware within the STM32Cube embedded-software packages or Standard Peripheral Library.

Complete article, here

Compact lens-less digital microscope – evaluation kit available

EDN Europe first reported on the work on lens-free microscopy at Belgian research centre imec in 2014. Now, the technique has been packaged into a demonstration and evaluation kit.
Able to provide a large field-of-view and live imaging at micrometer resolution, imec's on-chip lens-free microscope can be integrated into life sciences and biotech tools, targeting multiple applications such as label-free cell monitoring, automated cell culturing, or automated high-throughput microscopy. The principle behind lens-free imaging is based on in-line holography capturing the interference between an illuminating wavefront and the diffraction of an object. Selection of field of view; of magnification; and of plane of focus; all become software operations.
Compared to conventional optical microscopes, lens-free digital microscopy removes the need for expensive and bulky optical lens components to acquire and visualise microscopy images. In a lens-free digital microscope, images are captured on a CMOS image sensor, and digitally reconstructed using software. Imec's lens-free microscope features a comparable micrometer-scale accuracy as traditional optical microscopes, while being much smaller and less expensive; the microscope captures a larger field-of-view and enables a full-resolution selection to be achieved across a much wider field in one shot, enabling shorter sample processing times. The lens-free microscope paves the way to new applications with living cells and tissues.
"Imec's lens free imaging solution is now available as a full, ready-to-use demo kit evaluation system including a light source, image sensor, control and read-out electronics and a software interface," stated Jerome Baron, business development manager of integrated vision systems at imec. "Companies can use it to try out their own applications, supported by our engineers to fine-tune the hardware and software and customise the systems toward their exact application requirements."



Complete article, here

Rohde & Schwarz puts spotlight on cybersecurity, adds new division

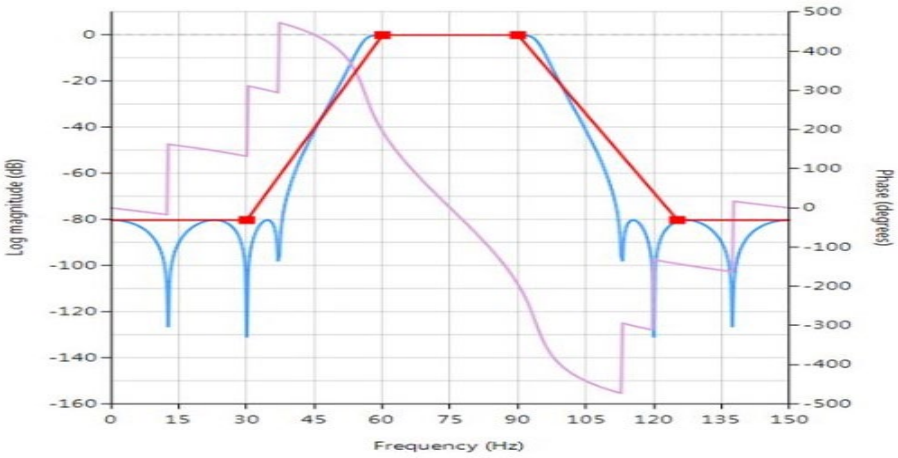
The communications and T&M company is to set up a specialist group that combines its IT and network security subsidiaries as 'Rohde & Schwarz Cybersecurity'. Rohde & Schwarz Cybersecurity will apply a new security-by-design technological concept to deliver proactive protection against outside attacks; the company has taken this approach to safeguarding data and communications in times of global networking, and is increasing its involvement in this future market.

Rohde & Schwarz has been active in the field of IT security for over 20 years. In 2014 and 2015, the group enhanced its know-how by acquiring **Adyton GmbH, gateprotect GmbH** and **Sirrix AG**. Long-standing subsidiaries **ipoque GmbH** and **Rohde & Schwarz SIT GmbH** will continue to contribute to the portfolio with their expertise and solutions. As part of the consolidation, Rohde & Schwarz SIT will be reorganised: its Stuttgart office will focus on its core business of radiocommunications encryption solutions. The end-to-end encryption and network security product groups will remain in Berlin. They will be integrated into Rohde & Schwarz Cybersecurity GmbH, which will have a total of nearly 400 employees at six locations in Germany. Rohde & Schwarz Cybersecurity offers a wide range of technologically leading solutions for information and network security. Highly secure encryption solutions, next-generation firewalls and software for network analysis and endpoint security protect enterprises and public institutions worldwide against espionage and cyberattacks. Security solutions range from compact, all-in-one products to customised solutions for critical infrastructures. The development of trusted IT solutions focuses on the new security-by-design technological concept for preventing external attacks proactively instead of reactively.

Complete article, here

Automated filter design package offers intuitive, graphical approach

Advanced Solutions Nederland has formally released version 3.0 of its ASN Digital Filter Designer. The company says that the package, for IIR and FIR filter design, offers an intuitive route to implementing digital filters that represents the first significant advance in this class of tools for many years. The tool is a Windows-based package that assists with design of filters, primarily for implementation on processor targets, but also supporting floating point desktop algorithm development: work in this space has focussed on biomedical applications. ASN contends that, although existing design tools in the market can produce good results, their roots often date back some way (decades, in some cases), they were conceived for use by an "expert" level of filter designer and considerable specialist expertise is needed to reach those results. ASN Digital Filter Designer has been structured to use an intuitive input approach that largely dispenses with entering parameters in text fields. Rather, it uses a GUI-based methodology in which the user draws the desired filter response (for classical filter configurations). For those classic designs, the tool will work directly from a graphical input to establish the necessary technical specifications for both IIR and FIR filters. Alternatively, the user can create customised designs by entering specifications as simple symbolic mathematical expressions and then interactively experiment-



ing with settings. The symbolic math scripting language allows exploration of complex designs.
The software supports detailed time and frequency domain analysis and a pole/zero editor to fine-tune a design. Outputs include full documentation and reports, and filter coefficients can be exported other environments (Matlab, etc.) for further analysis or development. IIR filter design can proceed with classical forms in lowpass, highpass, bandpass and bandstop configurations in Butterworth, Chebyshev Type I, Chebyshev Type II or Elliptic types, with filter orders of up to 100 (in the 'professional' version of the tool) supported. FIR (finite impulse response) filter design is implemented via the Parks-McClellan algorithm, and allows for the design of lowpass, highpass, bandpass, bandstop, multiband, Hilbert transformer, and differentiator filters with orders up to 500.

Complete article, here

Mentor proposes Open Manufacturing Language for PCB assembly

Mentor Graphics has launched the Open Manufacturing Language (OML) initiative that directly addresses what it terms the longstanding need and urgent calls from the industry for a printed circuit board (PCB) assembly-specific "Internet of Manufacturing", "Industry 4.0" solution.
For the first time – Mentor says – IT teams, solution providers, and equipment providers can integrate shop-floor data to create or enhance added-value manufacturing execution solutions based on a single, normalised, vendor-neutral communication interface. This minimises development and support effort while ensuring optimum data accuracy, timeliness and completeness.
Use of the OML standard supports numerous industry needs and challenges including the practical realisation of the Internet of Manufacturing, Industry 4.0 and Smart Factory 1.0 concepts, as well as the automated collection of full traceability data including routing and compliance enforcement.
OML creates an operational hierarchy through which neutralised information is exchanged between manufacturing processes. This includes detail of any shop-floor event in the areas of process performance, materials setup and consumption, traceability, process results and parameters, process control (poka-yoke), and quality information from test, inspection and repair processes, both automated and manual. OML resolves numerous issues in automated and manual processes that previous formats could not address.
The standard will be available through an open community on www.OMLcommunity.com. The community will provide support and management of new revisions. Membership of the community is now open for end-users, machine vendors, and other interested parties by registering at the website where a free download of the full documentation and samples are available.

Complete article, here

Untethered 3D dead-reckoning bridges gaps in automotive location fixes

u-blox' NEO-M8U is presented as the first Untethered 3D Dead Reckoning (UDR) module; combining multi-GNSS (GPS, GLONASS, BeiDou, Galileo) with an onboard 3D gyro/accelerometer, NEO-M8U provides accurate positioning even where GNSS signals are weak or not available. It achieves this without any connection to the vehicle other than power.

The u-blox NEO-M8U module provides superior multipath suppression, which improves position accuracy even in tough environments, such as urban canyons, tunnels, or parking garages. For example, in London's city centre area, NEO-M8U is typically three times more accurate than a traditional GNSS receiver. NEO-M8U offers instantaneous position immediately after power-up, without the need to wait for a first fix as with regular GNSS receivers.

Simplifying product development and installation, NEO-M8U looks and behaves just like a regular GNSS receiver and does not require any special mounting or connection to the vehicle. With intelligent sensing and continuous self-calibration, NEO-M8U can be installed in the vehicle in any orientation.

Complete article, here

Quad SPI FRAM at 4Mbit capacity

Fujitsu's ferroelectric RAM offers high speed non-volatile memory for networking, industrial computing and HMI applications. The company presents the MB85RQ4ML as the first-available Quad SPI FRAM device. It integrates 4 Mbit FRAM (Ferroelectric Random Access Memory) and Quad SPI interface. By using 4 bi-directional I/O pins, the Quad SPI FRAM device can reach a data transfer rate of 54 MByte per second at an operating frequency of 108 MHz. In this respect, the memory is over four times as fast as Fujitsu's existing parallel 4Mbit FRAM device and outperforms 45 nsec parallel SRAM. MB85RQ4ML comes in an SOP-16 package. In comparison to the company's parallel devices of the same density, which are housed in TSOP-44 or TSOP-48 packages, it achieves a package size reduction of at least 50% as well as a pin count reduction of 60%. Besides its high speed, The device offers the usual FRAM characteristics such as non-volatility and high endurance of 10 trillion read/write cycles. Since power is not required to retain the data written in the memory, MB85RQ4ML can replace battery backed-up SRAMs.

While the conventional memory architecture of embedded systems consists of a RAM and a non-volatile memory, it can, in many applications, replace both kinds of memory technologies and offer a unified memory technology in one chip.

MB85RQ4ML operates at a voltage range of 1.7 – 1.95V. As well as Quad SPI, single SPI interface is supported.

Complete article, here

Hardware cryptographic acceleration and secure storage for TLS in IoT apps

Atmel has disclosed a hardware interface library for TLS stacks used in Internet of Things (IoT) edge node applications. Hardening is a method used for reducing security risks to a system by applying additional hardware security layers and eliminating vulnerable software.

Atmel's Hardware-TLS (HW-TLS) platform provides an API that allows TLS packages to use hardware key storage and cryptographic acceleration even in resource constrained edge node designs. HW-TLS is a comprehensive solution pre-loaded with unique keys and certificates designed to eliminate the complexities of generating secure keys in the manufacturing supply chain.

OpenSSL is a general-purpose cryptography library that provides an open-source implementation of the Secure Sockets Layer (SSL) and TLS protocols. wolfSSL is a cryptography library that provides lightweight, portable security solutions with a focus on speed and size. Atmel's ATECC508A-OpenSSL and ATECC508A-wolfSSL are available for immediate download at their respective software distribution repositories, offering seamless adoption of more secure elements without disruption to the developer workflow.

Secure hardening for both OpenSSL and wolfSSL is made possible with HW-TLS which allows those TLS software packages to interface seamlessly with the Atmel ATECC508A CryptoAuthentication co-processor. The ATECC508A provides protected key storage as well as hardware acceleration of Elliptic Curve Cryptography (ECC) cipher suites including mutual authentication (ECDSA) and Diffie-Hellman key agreement (ECDH). As such, HW-TLS allows developers to substantially harden Transport Layer Security (TLS), enhancing security for IoT-device and cloud-service ecosystems.

When used together, HW-TLS and the ATECC508A allow even extremely small, low-cost IoT nodes to implement strong cryptographic security. All private keys, certificates and other sensitive security data used for authentication are stored in secure hardware and protected against software, hardware and back-door attacks. In addition, the integrated ECC accelerators in the ATECC508A offload cryptographic code and math from the MCU allowing even a low end processor to perform strong authentication.

Complete article, here

Rohde & Schwarz 2 GHz scope offers linked multi-domain views

Rohde & Schwarz' RTO2000, is a compact lab oscilloscope for multi-domain applications, displaying correlations between time, frequency, protocol and logic analysis measurement results.

Via the analogue input channels, the user simultaneously sees the signal in the time and frequency domain, and if desired, the spectrogram. Newly added functions such as peak list, max. hold detectors and the logarithmic display make frequency analysis more efficient.

A zone trigger enables the graphical separation of events in the time and frequency domain. Users can define up to eight zones of any shape. A trigger signal is activated when a signal either intersects or does not intersect the zone. This makes it easy to detect disturbances in the spectrum during EMI debugging or to separate read/write cycles of storage media in the time domain.

It is the first oscilloscope in this class to offer a memory of up to 2 Gsample/sec. This is useful for the history function, which provides access to previously acquired

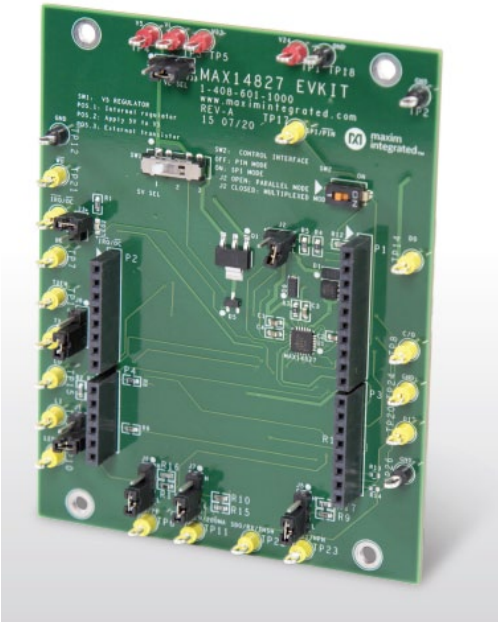
waveforms at any time. A trigger timestamp allows time correlation. Users can view all saved signals and analyse them with tools such as zoom, measurement, math and spectrum analysis functions. Signal processing in the ASIC and intelligent memory management ensure smooth handling of long pulse and protocol sequences.
A high definition (HD) mode increases the vertical resolution to up to 16 bits, making signal details visible. Achieved by signal processing, the high-resolution mode trades bandwidth for increased detail. The HD mode activates configurable lowpass filtering of the signal after the A/D converter.
With one million waveforms per second, the R&S RTO2000 enables users to detect sporadic signal faults. The scope provides high-speed analysis even when histogram and mask functions are active. The R&S RTO2000 is available as a two or four channel model with a bandwidth of 600 MHz, 1 GHz, 2 GHz, 3 GHz or 4 GHz, priced from (approximately) €15,000 to €50,000 depending on configuration and bandwidth.

Complete article, here

3rd-generation IO-Link transceiver chip cuts power, package outline

Maxim Integrated's MAX14827 enables intelligent sensors with reduced maintenance and increased uptime with continuous diagnostics and monitoring; it reduces power dissipation more than 50% over prior devices.
Industrial systems designers, Maxim says, now have a robust IOLink dual-channel transceiver that dissipates the lowest heat in the smallest package; IO-Link sensors contribute to the 'Industry 4.0' trend by bringing intelligence and control down to the factory floor.
Sensors are getting smaller and need to deliver more functionality, while ensuring robust communications: power – says Maxim - is also critical because these sensors are small and it is difficult to dissipate heat. The MAX14827 dual-channel, 250 mA transceiver meets these requirements, while also integrating high-voltage functions commonly found in industrial sensors, including drivers and regulators.
It features two ultra-low power drivers with active reverse-polarity protection to reduce downtime. For sensors that use a microcontroller, a SPI interface is available with extensive diagnostics. For IO-Link operation, a three-wire UART interface is provided, allowing interfacing to the microcontroller UART.
A multiplexed UART/SPI option allows using one serial microcontroller interface for shared SPI and UART interfaces. The device includes on-board 3.3V and 5V linear regulators for low-noise analog/logic supply rails.
Advantages include; a lower on-resistance (RON): 2.5 Ohm Ron (typical) saves more than 50% power; the WLP package saves 60% space; a 65V Abs Max rating enables flexible TVS protection selection.

Complete article, here

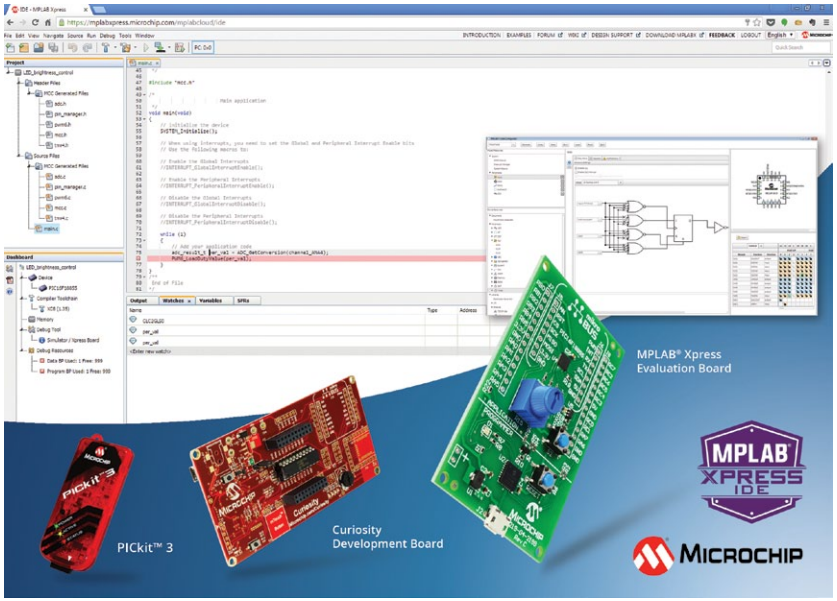


Free, cloud-based development platform; entry to the world of PIC

Way before the world learned that they were called 'makers', experimenters and product developers working around the boundary between the professional and semi-pro, even hobbyist, worlds could very often be found using Microchip PIC devices; now, the company has updated the entry path it offers to that group of users – and to the 'regular professional' sector that may not be familiar with PICs – to take account of online, cloud-based trends.

The offering is called MPLAB Xpress IDE and Microchip says it provides the "easiest way to get started with PIC MCUs". It allows you do a considerable amount of work on a project without even registering ("no downloads, sign-in or setup required to start") It is an online, cloud-based development environment, the only one, Microchip says, with an integrated Code Configurator. You can pair it with hardware in the form of existing Microchip MPLAB boards, or with any PC plus the new MPLAB Xpress Evaluation Board – numbers of these (see below) are going to be in circulation via free hand-outs and if you miss out on those; for under $10.

The platform gives access to the entire family of PIC MCUs – initially, all 8-bit variants, with 16-bit parts to follow later in 2016. The 'first encounter' is a free login to the site; that gives access to examples, code libraries and compilation – and to a code configurator (code generator) to set up a chosen target and its peripherals. A free account setup allows you to save work to the cloud, with the option of making work 'open' or visible to a community.



Designers can, therefore, create an application, simulate, compile code, programme and debug an MCU in this cloud-based toolset which inherits the most popular features of the MPLAB X IDE. MPLAB Xpress offers a comprehensive feature set, including a library of Microchip-validated code examples, interface to MPLAB Code Configurator (MCC) 3.0 for GUI-based MCU peripheral setup and automatic code generation, integrated MPLAB XC compilers, support for programmer/debugger hardware, and 10 GB of secure online storage with a myMicrochip account. Users can easily migrate their projects to the full, downloadable MPLAB X IDE. A new MPLAB Xpress Community enables developers to share their code, design ideas and knowledge.

Cloud-based hardware development is supported by connecting any USB-enabled PC, laptop or tablet to tools such as the MPLAB Xpress Evaluation Board. This development board features an integrated programmer, a PIC16F18855 MCU and a mikroBUS header for system expansion with MikroElektronika's more than 180 Click boards. The MPLAB Xpress IDE also supports Microchip's Curiosity Development Board ($20.00), with integrated programmer and debugger, as well as expansion options for add-on boards and external connectivity. The online IDE can be used with Microchip's PICkit 3 In-Circuit Debugger/Programmer ($47.95), which provides programming and debugging capabilities for over 1,000 PIC MCUs.

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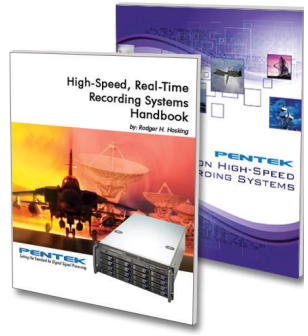

TALON

THREE WAYS TO REDUCE UNCERTAINTY AND IMPROVE NOISE FIGURE MEASUREMENTS

Cherisa Kmetovicz, Keysight Technologies

Noise figure (NF) is a key parameter in the performance of RF receivers and systems. It measures the degradation in the signal-to-noise ratio (SNR) as a signal passes through the device under test (DUT). A receiver with a low noise figure has the capability to detect low-amplitude signals, and this directly correlates to improved bit error rate (BER) in a digital communications system.

The process of reducing noise figure starts with a solid understanding of the uncertainties in the receiver—its components and subsystems—and the test setup. Quantifying those uncertainties depends on flexible tools that provide accurate, reliable results.

Use an NF uncertainty calculator

The calculation of uncertainty can be complex and time-consuming, but it becomes simpler and faster with the many calculators available. The right choice depends on the chosen technique, and the most common choice is the Y-factor method. This uses two pieces of equipment: a calibrated noise source to provide a stimulus to the DUT input and a signal analyzer to serve as a calibrated receiver that measures the DUT's output noise.

The noise source is specified with an excess noise ratio (ENR) that characterizes the on and off noise power as a function of frequency. Because ENR uncertainty is a main contributor to overall NF uncertainty, it is included in the NF calculation. Other contributors include mismatch, gain linearity and the analyzer's own noise figure.

Table 1 illustrates the contributors to uncertainty for a low-noise 6 GHz amplifier with a 3 dB NF, 26 dB gain and a voltage standing wave ratio (VSWR) of 1.5. The noise source had an ENR uncertainty of ±0.078 dB and a VSWR of 1.05, and the main contributors to total measurement uncertainty were ENR uncertainty at 88 percent and mismatch at 12 percent.

Contributor	Percentage of total uncertainty
ENR uncertainty	88%
Mismatch	12%
Gain linearity	< 1%
Analyzer noise figure	< 1%

Table 1. *Two factors dominate the NF measurement uncertainty for a 6 GHz low-noise amplifier.*

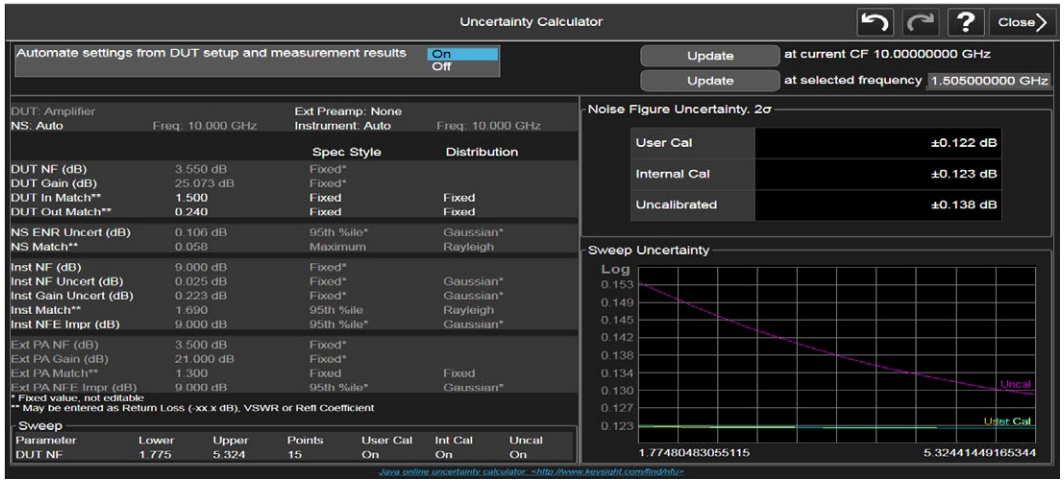

Figure 1. *As implemented in the NF application, graphical and informational results are presented on the screen of the EXA signal analyzer.*

Noise source	Noise source ENR uncertainty	Noise source VSWR	DUT NF uncertainty
Smart noise source (SNS)	±0.087 dB	1.05	±0.112 dB
Typical noise source	±0.180 dB	1.25	±0.213 dB

Table 2. *A smart noise source provides much less measurement uncertainty.*

Adding up the components produced an uncertainty of ±0.112 dB. This implies that an amplifier with a 3 dB noise figure would yield a measured value between 2.888 dB and 3.112 dB.

The fastest way to calculate uncertainty is to use a signal analyzer equipped with an NF measurement application. One example is the Keysight EXA X-Series signal analyzer (N9010B) and the N9069C noise figure application, which provides one-button operation and includes a built-in uncertainty calculator.

For the active measurement, the calculator reports total NF uncertainty on the instrument display. For example, the uncertainty calculator screen reports total measurement uncertainty along with a graph of uncertainty versus a swept parameter (e.g., DUT NF, gain or match).

Select a noise source with low uncertainty

Because ENR uncertainty has the largest effect on total measurement accuracy, it's important to use a noise source that has the lowest uncertainty for a specific application. One example is a Keysight SNS Series smart noise source, which automatically downloads electronically stored calibration data to the analyzer. It also automatically measures its own temperature so compensation can be applied to the calibration data. These noise sources provide less uncertainty than can be obtained with most standard noise sources. Table 2 provides a comparison.

Use a smart preamplifier

Adding a preamplifier to the test setup will improve the NF performance of the signal analyzer. The preamp can be either internal to the analyzer's signal path or an external unit that is inserted between the DUT output and the analyzer input (Figure 2).

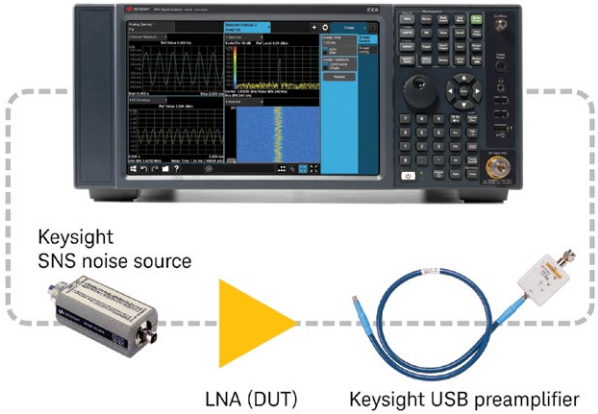

Figure 2. *Keysight instruments, applications and accessories work together to provide accurate, reliable NF measurements.*

External smart preamplifiers automatically download calibration information to the analyzer via USB and improve NF performance. Keysight's smart preamps provide gain correction with temperature compensation, and are also optimized to flatten the analyzer's frequency response and thereby reduce measurement uncertainty.

Conclusion

A robust solution set for noise figure measurements—instruments, applications, and accessories—simplifies the process of optimizing test setups and identifying unwanted sources of noise. The use of a one-button measurement application, a built-in uncertainty calculator, a low-uncertainty noise source, and a smart preamp will accelerate the process and improve measurement results.

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REDUCING TEST TIME AND COSTS WITH NEW COMPRESSION TECHNOLOGY

By Mike Vachon, Software Engineering Group Director, Cadence

Every working chip that comes off a production line spends part of its time on automated test equipment (ATE), where its memories, chip I/O interfaces, analogue circuitry, and digital logic are carefully examined. Typically encompassing 10-50% of total test time, testing of digital logic can represent a significant portion of overall product cost.

All told, testing is a costly, yet critical, part of the overall chip development process, with the industry spending roughly $4 billion annually on ATE. And as chip designs continue to grow in size and complexity, particularly at advanced nodes, test costs will only continue to go up.

We've seen various cost-reducing test technologies rolled out by the Design for Test (DFT) community over the years, but nothing deserving the description of a breakthrough in the last 15 to 20 years. Today, XOR-based test compression, typically providing compression ratios of 50- to 100-fold, remains the most widely used. XOR compression reduces test time by partitioning registers in a design into more scan chains than there are scan pins on the chip to connect to the ATE.

At process geometries of 16nm/14nm, however, SoC designers are finding that they need to go beyond 100X compression in their scan vectors in order to control test cost and avoid having to spend money buying additional testers. Clearly, the market is ready for a new way to minimise test costs.

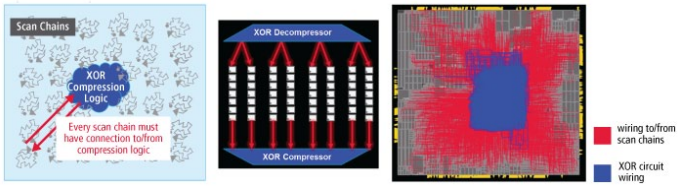


Figure 1. *Wiring overhead associated with compression logic.*

Limitations of traditional XOR compression

As the ratio between the number of scan chains and the number of scan pins increases in a traditional XOR compression architecture, the length of each scan chain decreases, resulting in fewer clock cycles to shift-in each test pattern. For a constant pattern count, fewer shift clock cycles per pattern requires less total test time on the ATE – hence the test cost savings advantage.

Fewer clock cycles per pattern also means fewer bits of information in each pattern to control register values and detect faults. In this scenario, a higher compression ratio becomes problematic. Should the compression ratio become too high, the achievable fault coverage drops because some faults will need more register values to be controlled than there are bits in a test pattern. Even if fault coverage can be maintained, as the compression ratio goes up, the number of patterns needed to maintain this coverage increases rapidly because it becomes more difficult to pack the detection of multiple faults into a single pattern. Ultimately, increasing the compression ratio results in a diminishing benefit on total test time. In addition, a higher compression ratio results in a substantial impact on the physical implementation of a chip—after all, every scan chain has to be connected to and from the XOR compression logic (as shown in Figure 1).

At a typical compression ratio of 100X, the average impact on total chip wiring resources of an XOR codec across a range of common digital components is in the range of 3-5%. What if you attempted to increase the compression ratio to 400X, particularly to meet the test needs of advanced-node designs? … *article continuation: click for pdf*

IT'S NOT JITTER, IT'S NOISE

BY RANSOM STEPHENS

An oscilloscope draws a two-dimensional view of a signal – voltage versus time. In this column, let's ponder noise in these two dimensions.

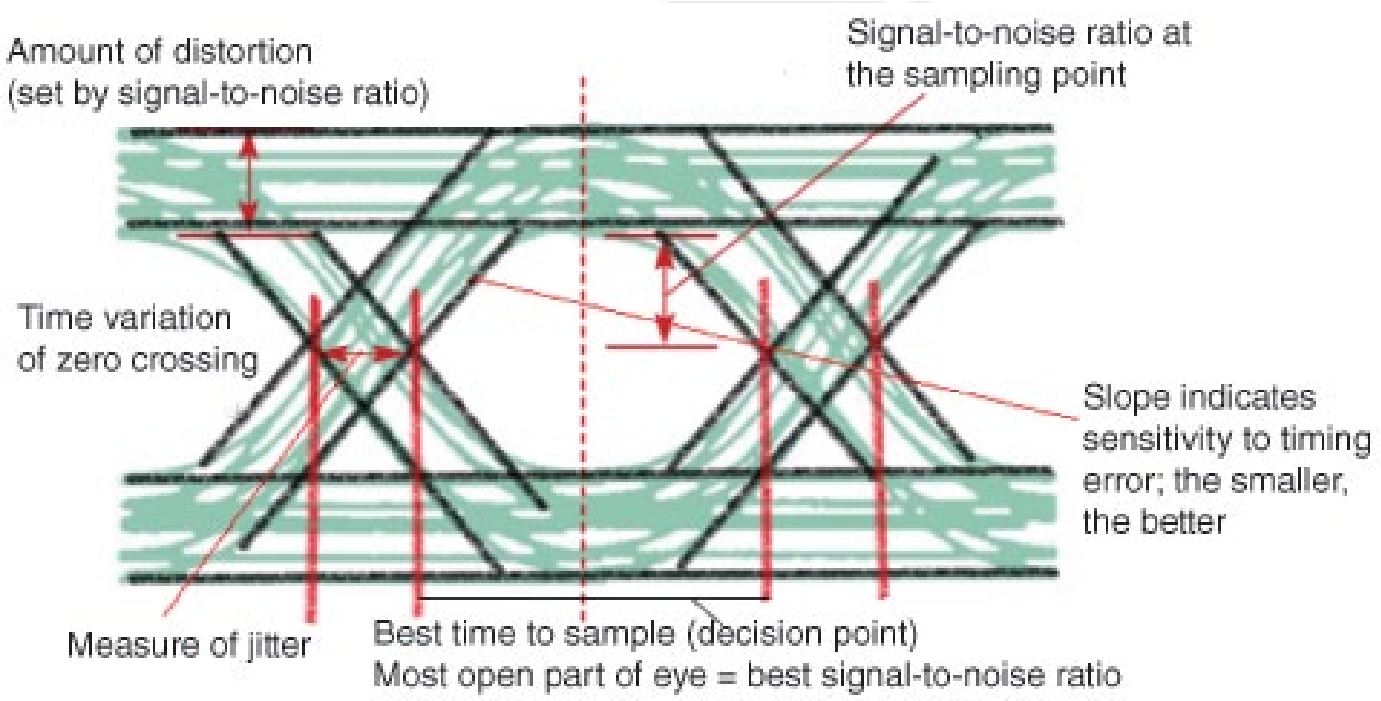
When we look at a digital signal on a oscilloscope, the only noise we care about is noise that causes errors. In high-data-rate signals, the vast majority of errors occur when the timing of a logic transition fluctuates across the sampling point. That sampling point should be close to the centre of the eye. For a differential signal, it's right around (t, V) = (n+½T, 0), where n is an integer, and T is the bit period.

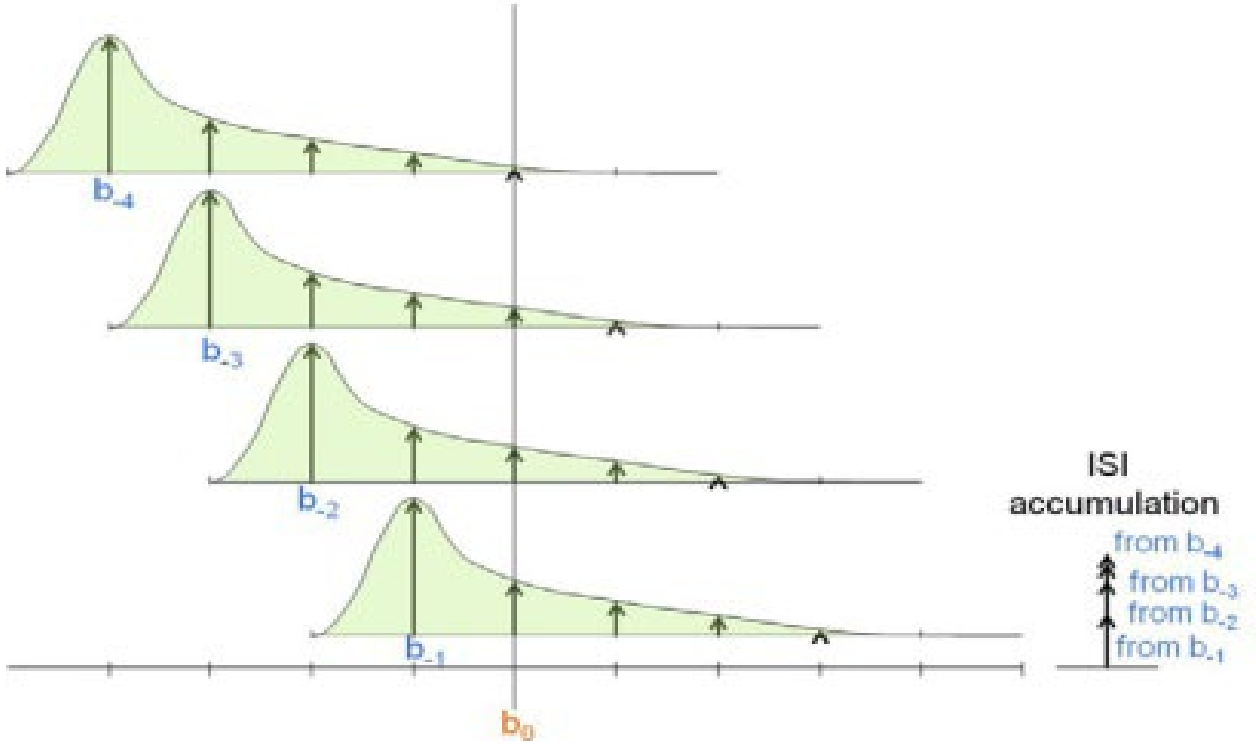
If transitions had zero rise/fall time, jitter caused by phase noise would be the sole culprit. But voltage noise shifts edge timing, too.

Consider the rising edge of a 0-to-1 transition. If, for example, voltage noise pushes the edge down, then the time position at V=0 shifts to the right. If the rise time and voltage noise are large enough, the edge shifts past the sampling point, and what should have been a 1 is mistaken for a 0.

In high-speed serial systems, the channel is the dominant cause of eye closure. The channel acts like an attenuating low-pass filter. Rise/fall times increase as higher-frequency components are damped out. The effect is called intersymbol interference (ISI), because the shape of a particular bit in the waveform is affected by the frequency content of bits that surround it. For example, a sequence of alternating ones and zeros has higher-frequency content then a long string of identical bits.

The combination of more gentle edges and reduced peak-to-peak voltage causes errors in two ways. First, the gentle-sloping edge of a transition might pass right by the sampling point. Second, a transition may never be higher or lower than the sampling-point voltage. The amplitude of a 1-to-0 transition that follows a long string of identical bits may not drop below the sampling point through the entire bit period.





A more interesting point (and, as 100-Gigabit Ethernet emerges, an increasingly relevant one) is crosstalk-induced jitter. Crosstalk is electromagnetic interference (EMI) generated by logic transitions of one signal, the aggressor, and picked up on the trace of another, the victim. The magnitude of the pickup depends on the victim-aggressor mutual inductance.

Both ISI and crosstalk cause jitter, but they are voltage noise, not timing noise.

Of course, equalisation was invented to defeat ISI. It's easy to amplify the high-frequency signal components that ISI damps out. You can do it at the transmitter with de-emphasis or at the receiver with a continuous time linear equaliser (CTLE), in either analogue or digital form, or with a linear feed forward equaliser (FFE).

It's worse for crosstalk, though. Simple equalisation techniques can open eyes closed by ISI, but to a receiver, crosstalk looks like randomly occurring blasts of noise. No simple, linear equalisation technique can reduce the effects of crosstalk. Depending on the relationship between the underlying clocks of the victim and the aggressor, decision feedback equalisers (DFEs) can help.

In both cases, to understand how both voltage and timing noise affect your system, don't overlook noise analysis in your headlong rush to jitter analysis. Most advanced oscilloscope jitter analysis software includes noise analysis. Another way is to expand the two-dimensional V(t) analysis of an oscilloscope to three dimensions with a bit error rate (BER) tester or a BERTscope and look at BER(t, V), also known as the BER contour.

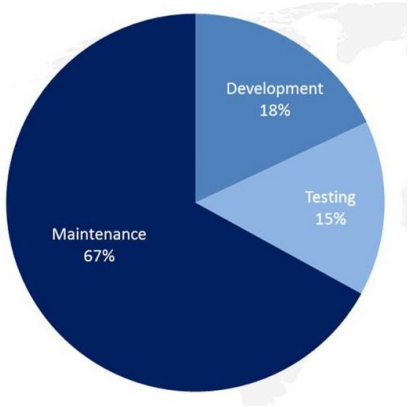
PAYING DOWN TECHNICAL DEBT

By John Paliotta, Vector Software

In last month's edition, John Paliotta introduced the concept of technical debt; the burden we impose on systems in the form of latent defects introduced during system architecture, system design, or system development. In this second part of the discussion he looks at how – like all who have over-indulged in tempting credit – we can begin to pay back the debt and, especially, to prioritise which parts of the debt mountain to attack.

Technical Debt is a great metaphor for the latent bugs and ugliness that exists in all of our code bases. There have been lots of advances in software development processes over the last 30 years, but the quantity of software being developed has far outpaced our ability to build quality software efficiently.

Cambridge University estimates that the global cost of debugging software is $312 billion annually. Software publishers are under constant pressure to release new products and new features quickly, which often causes a conflict between quality and time-to-market, as release cycles shrink from years to weeks to days.



Lots of money is being spent on the problem; Cambridge University estimates that the global cost of debugging software is $312 billion annually; and an accepted ratio is that maintenance costs are generally double the original development and testing costs.

In this article we'll discuss practical ideas for reducing technical debt in our legacy code bases; which will increase quality, reduce maintenance costs, and allow us to deliver new functionality to our customers, faster.

How did we get here?

Technical debt is not new, nor is it all bad. We rarely have the time to build the perfect product, or the perfect software application: there are always trade-offs.

Software is very malleable, it is easy to change, which makes it easy to break. Most software exists in a constant state of flux; you start with a nice clean design, but that design gets corrupted as changes are made to fix bugs and implement new features. Without constant vigilance and refactoring, software applications get ugly over time.

Years ago when software applications were much smaller, the solution to ugly applications was a complete re-write. When the average application was only 50,000 lines of code – it was easy enough – or, at least, feasible – to throw them away and create a new implementation.

With modern application sizes in the millions of lines of code this is no longer an option, incremental improvement is the only option.

Understand the problem

To understand where technical debt may be building up, it is important to look at metrics.

The top four causes of technical debt are: poor architecture, overly complex code, inadequate testing, and lack of documentation. So the first step is to capture key metrics related to these issues: cyclomatic complexity, source code coverage, and comment density. *...article continues, click for pdf*

USING COMMUNICATIONS SEMICONDUCTORS TO COOK BETTER BURGERS

By Robin Wesson, Ampleon

The ubiquitous microwave oven is about to be revolutionised by the application of solid-state RF electronics and signal-processing techniques borrowed from the communications industry and applied to what, for many households, will be their last vacuum-tube-based appliance.

Improvements in the power output and efficiency of solid-state RF amplifiers mean they can now replace the resonant-cavity magnetrons that have been used in microwave ovens since they were launched 70 years ago. This will bring designers new ways to control how these ovens cook our food, and provide consumers with better burgers and "perkier pancakes". The same enhanced control of heating, and precision of results, is also available to designers of systems that use microwave heating as part of an industrial or manufacturing process.

How is this possible? After decades of development, magnetrons generate high-power RF signals with good efficiency at relatively low cost. However, the output frequency of this valve technology varies, its performance changes with temperature, and it is not possible to control its amplitude or phase accurately.

You can see the result in Figure 1, which shows an oven heating the same load for 30s, three times over. It's hard to deliver consistent cooking on the basis of such variability.

There are two further issues with microwave cooking, regardless of the RF source used. The first is that the way that RF energy is absorbed depends on its frequency and the dielectric properties of the food. This means that, for consumer microwave ovens operating around 2450 MHz, food is only directly heated to a depth

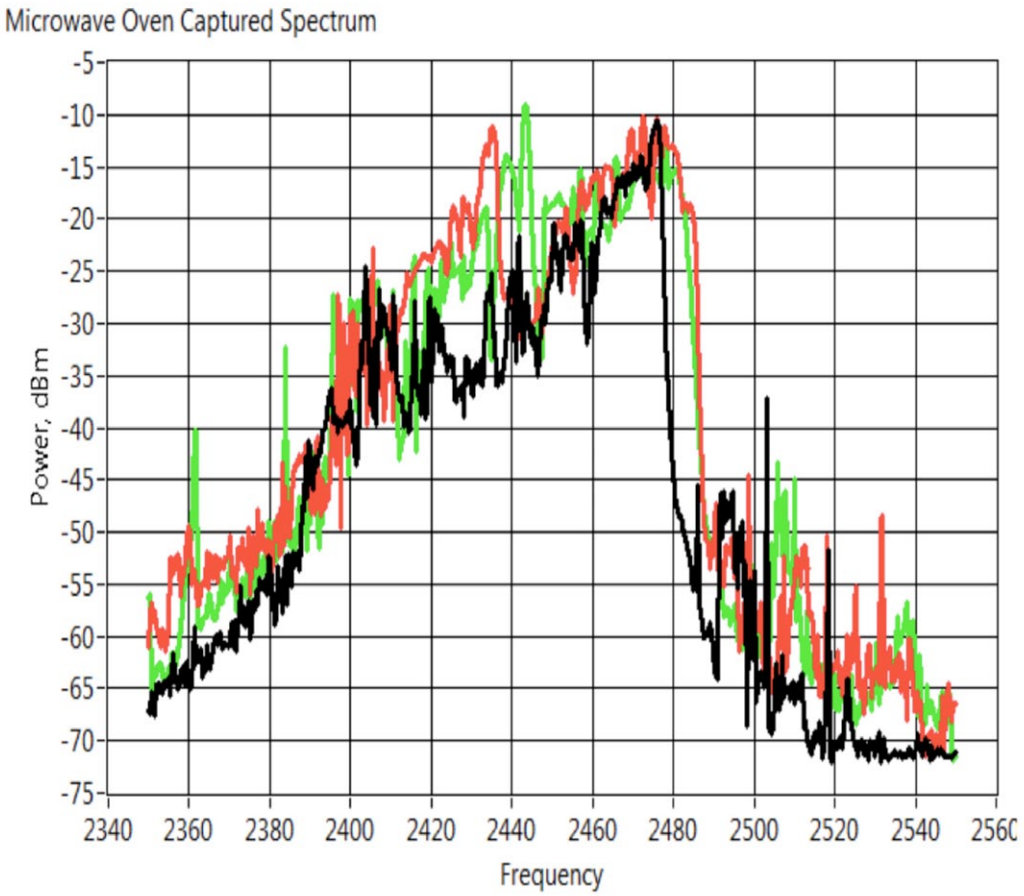


Figure 1. *Magnetron spectral emissions in microwave oven operation – 3 traces of 30 seconds captured from the same oven with the same load (Source: Ampleon)*

of a couple of centimetres. The second issue is that microwave energy from the source interacts with the cavity to set up standing waves with local energy maxima and minima, which in turn create hot and cold spots in the food being heated.

The fact that the standard measure of a microwave's utility is its ability to heat a litre of water has done little to encourage designers to develop ovens that work well on real food.

The innovation opportunity

The communications industry has been developing and using high-power RF components for decades. Communications system designers also face issues, such as delivering enough signal energy to users in complex multipath environments, which are surprisingly similar to those of a microwave oven designer – although the scale is different.

So what techniques can microwave oven designers borrow from their communications industry colleagues, and what opportunities for innovation would they bring? Let's examine a few of these.

Power control

The amount of energy delivered to the food in today's microwaves is controlled by turning the magnetron on and off - a basic form of pulse-width modulation (PWM). The switching rate is limited by the time it takes for the magnetron to reach its operational temperature, which can result in poor cooking results due to thermal cycling at the edges of some foods.

Solid-state systems can handle PWM control with periods measured in microseconds, not the seconds necessary for magnetrons, making it possible to deliver energy in a more linear fashion. In effect, the flexibility of a solid-state power delivery gives microwave users the same control of power delivery that we take for granted from an electric oven or gas grill. The solid-state approach offers one more advantage - variations in the power and gain of the source can be corrected with a closed-loop control system, improving repeatability. *The article continues, considering the application of feedback and frequency/phase control- click for pdf.*

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NEW GENERATION OF PHYSICAL RTL SYNTHESIS IMPROVES QUALITY-OF-RESULTS

By Arvind Narayanan, Mentor Graphics

The quality of the netlist generated during RTL synthesis has an enormous impact on the rest of the physical design flow. For teams designing large SoCs at advanced nodes, it is more important than ever to come out of RTL synthesis with predictable timing and congestion estimates, DFT, and even a floorplan with good pin placements and feedthroughs. The quality of the netlist coming out of RTL synthesis has a big impact on the speed and predictability of the backend physical implementation and signoff.

What does quality of the netlist mean, and what are the bottlenecks of getting a good quality netlist for physical implementation? One barrier to better quality of results (QoR) from synthesis is when the synthesis tool optimises the design after generating gates from the RTL. For the best quality, designers need a high-capacity, physically-aware logic synthesis tool that optimises at a higher level of abstraction, not at the gate level. There are far more opportunities for QoR improvements when synthesis optimisation is performed at the RTL level.

However, there is a lack of physical information at the RTL level. Resorting to wire load models causes sub-optimal QoR metrics for

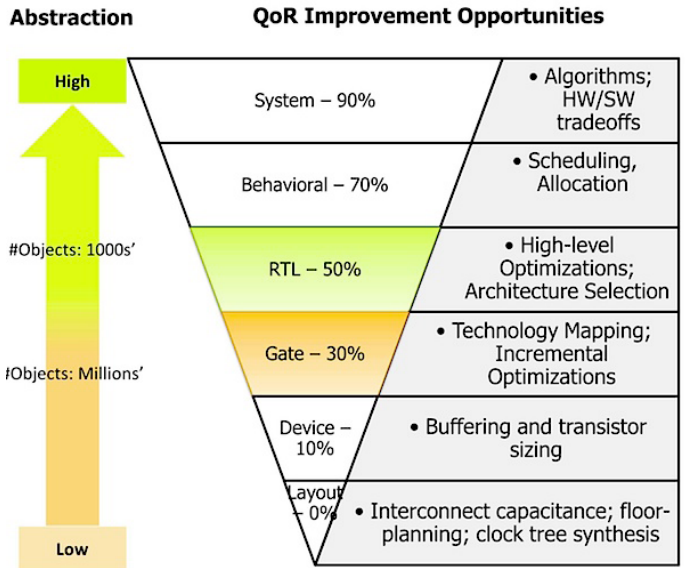

Figure 1. *Optimising at the RTL level offers more room for QoR improvement than gate-level optimisation, in addition to enabling higher capacity and faster runtimes.*

timing and congestion. The answer is to perform placement before synthesis so that high-level optimisation can be performed at the RTL level instead of the gate level, as with traditional synthesis tools. The new RTL synthesis tool should be able to divide the RTL into virtual placeable partitions and then refine those down into actual library cells so that physical placement information is available at all times. A detailed netlist of each RTL partition should be used to accurately time the design. Each partition should be optimised and implemented as placed gates and if needed, the RTL should be repartitioned until all top-level design specifications are met. The placement and timing information should be dynamically updated with every optimisation transform. This will result in a very tight correlation between RTL synthesis and place and route for timing and congestion.

The second barrier to QoR is that restricted tool capacity forces designers to break down their chips into smaller blocks for synthesis, and then re-stitch during physical design implementation. Breaking the design into blocks that don't correspond to the physical hierarchy is a recipe for disaster as it is very difficult to get a good partition, and hard to budget timing constraints across the blocks. The problem with this block-level synthesis approach manifests as endless iterations when assumptions made in the synthesis tool, which can only see a single block at a time, are invalidated by the physical design tool when all the blocks are considered as a group. The design that emerges from place and route no longer satis-

fies its constraints resulting in a mis-correlation between front- end and back-end design flows. Particularly for large designs, RTL and physical engineers should look for a tool with the capacity to perform true chip-level synthesis and floorplanning.

A side benefit of having high-quality physical RTL output is that it makes the entire design flow more predictable with shorter design cycles. Optimising at a higher level reduces RTL synthesis runtime, gives faster design convergence and cuts the time-consuming iterations. Using a high-level RTL physical synthesis solution with the capacity to handle 100+ million gate designs will deliver an enormous increase in productivity.

The third barrier to QoR is the general lack of robust what-if analysis during RTL synthesis. With a newer-generation RTL synthesis tool, designers can cross-probe between physical and RTL databases to debug timing or congestion problems. They can also perform parallel explorations of different design metrics, for example, varying the weight of power, performance, timing, DFT, and area to find the best alternative for implementation. The tool should be able to perform multiple fast synthesis runs with the different constraints for voltage, clock speed, and library, and gives the results in a comprehensive summary format.

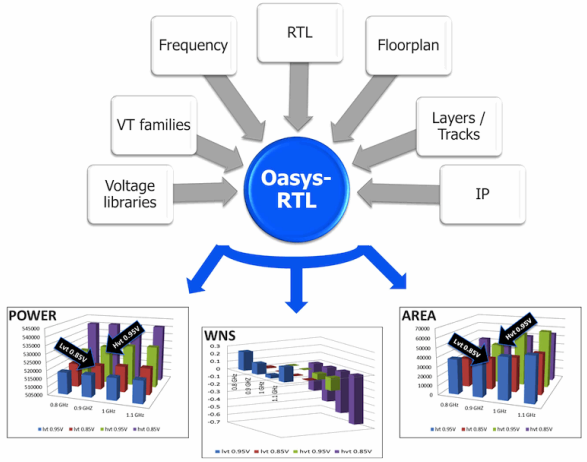

Figure 2. *Fast design-space exploration enables the designer to check and modify the design to meet timing, power, area, congestion, and DFT specifications.*

A final thought on design quality is the importance of chip-level DFT. Testability is increasingly difficult and undeniably important. Selecting DFT friendly architectures early and performing scan insertion at the full-chip RTL level helps reduce test time and limits the impact of test logic on die size. Physical RTL synthesis takes into account the physical location of flops when creating scan chains. Working at the chip level is better than working at the block level and then manually hooking up the sub-chains. Performing scan insertion during synthesis also lets potential test problems be debugged early in the design cycle.

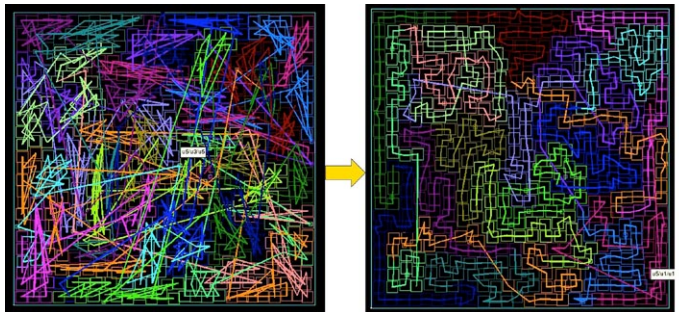

Figure 3. *The screen shot on the left shows a design in which the scan chains have not been ordered with their physical placement taken into account. The screen shot on the right shows the same design re-implemented using the physical placement information. Each scan chain is a different colour so the advantage in terms of routing is clear.*

Good RTL synthesis is critical for improving the performance, power, and area challenges in today's large advanced-node SoCs. A next-generation physical RTL synthesis tool must have higher capacity, faster runtimes, and better QoR than what's available in traditional synthesis solutions. Learn more about the concepts described here in the [Mentor Graphics] Oasys physical RTL synthesis white paper.

ATTAINING FUNCTIONAL SAFETY IN MCU-BASED DESIGNS

By Hoiman Low, Texas Instruments

In the 1980s, the use of programmable electronic components such as microcontrollers (MCUs) and microprocessors in industrial control systems began to grow. The International Electrotechnical Commission (IEC) set up study groups to examine the functional safety of electronic programmable systems and to develop guidelines for the development of safe systems. Since then, compliance to functional safety standards has become a customer-influenced requirement for end equipment developers in automotive and many industrial applications.

Standards, certification, and the development process

The first standard intended to apply to a wide variety of industrial systems was the IEC 61508 first edition, "Functional safety of electrical/electronic/programmable electronic safety-related systems," published in 1998. In 2011, the automotive functional safety standard ISO 26262 "Road vehicles — Functional safety" was published. The purpose of both standards is to establish requirements that reduce potential risk of physical injury and damage to the health of people due to product failure. They call for implementing a robust development process, performing upfront hazard and risk

Standard	System	Safety Integrity	Architectural Metric	Architectural Requirement	Failure Rate	Specific MCU self-test requirements
IEC 61508	Programmable E/E systems	SIL – 1,2,3,4	SFF	HFT>0 for SIL 4	PFD, PFH	No
ISO 26262	Automotive	ASIL – A, B, C, D	SPFM / LFM	No	PMHF	No
EN 50129	Railway	SIL- 1,2,3,4	N/A	Follow IEC 61508	THR	CPU, Memory
ISO 22201	Elevator	SIL – 1,2,3	N/A	Dual channels for SIL3	N/A	CPU, Memory, Interrupt, Clock, I/O, Comm
IEC 61800	Drive	SIL – 1,2,3 SIL4 Apply IEC 61508	SFF	Dependent on function	PFH (no PFD)	No
IEC 62061	Machinery	SIL – 1,2,3 SIL4 Apply IEC 61508	SFF	Supports ISO 13849 categories	PFH_D	No
IEC 61511	Process Automation	SIL – 1,2,3 SIL4 Apply IEC 61508	SFF	See IEC 61508	PFDavg	No
ISO 13849	Machinery	PL a,b,c,d,e	DC_{avg}	CAT B,1,2,3,4	$MTTF_D$	No
IEC 60730	Home Appliances	Class A, B, C	No	Yes (Class C)	No	CPU, Memory, Interrupt, Clock, I/O, Comms

Figure 1. *Safety standards.*

analysis, and implementing product risk reduction in both hardware and software.

IEC 61508 and ISO 26262 share a common functional safety lifecycle and many of the same supporting processes. Many other industry safety standards leverage these two, typically following IEC 61508 for reference adding specific architectural and self-test requirements for each particular system. Fig. 1 shows a summary of the various functional safety standards and their relationship with IEC 61508.

For a design to claim compliance to IEC 61508 and ISO 26262 functional safety standards, there must be a functional safety assessment of the end equipment, including any functional-safety-critical components used in the design that claim to comply with these standards. The end equipment assessment must be independent of the design team, and the level of independence is defined by the applicable functional safety standards. The end equipment assessment can be performed by an independent workgroup within the end equipment company, for instance, or by an independent third party certification agency. Exida, various Technischer Überwachungs-Verein organisations (known as TÜV), and Underwriters Laboratories (UL) are among the authorities offering such services.

But achieving effectiveness is more than performing end-product functionality development. End products must be developed using effective and necessary safety mechanism(s) to minimise the likelihood of failure occurring that would cause harm and include in the product built in mechanisms that facilitate a safe and predictable state when a product does fail.

Attaining safety certification

For customers who are new to functional safety standards, it is challenging to understand what it takes to apply functional safety standards and how to get end equipment certified. Here are some tips:

Certification agencies focus on three aspects of design:

- Company safety culture and the product development safety life cycle, including the development process and its supporting processes
- Management of random failures of a product

Certification agencies will look for documentation confirming that the end product was developed using processes to help mitigate sufficient failure risk reduction in compliance to the individual functional safety requirements.

The first design aspect can be stated as; A company’s safety culture and its development and supporting processes

Safety starts at the top. Senior management needs to empower its team to think about safety first and foremost. This means that employees will need to be appropriately trained on the applicable functional safety standard(s) (from Figure 1) and the company's system, hardware, and software development processes will need to be established to ensure compliance with applicable functional safety standards. Supporting processes such as change management, configuration management, verification, and validation need to be in place as well, along with normal quality system requirements such as TS16949, ISO 9001, etc.

Experienced functional safety teams strongly recommend that companies new to developing functional safety products work with a certification agency such as exida, TÜV, or UL, or a consulting service company such as kVA or Yogitech, to perform a gap analysis of their company’s safety culture, development, and supporting processes versus the functional safety standard requirements. The closure of early identified weaknesses and gaps will greatly facilitate the product development and ease certification in the long-run.

Safety-certified MCUs

Functional safety standards are typically applied to the Electrical/Electronic/Programmable Electronic Safety-related System (E/E/PES) elements of a product. During certification, a certification authority examines evidence of product development to determine if these

elements are in compliance with the functional standard requirements. As a key component in many E/E/PES systems, MCUs will be especially scrutinised.

Frequently asked questions regarding MCUs are:

- Is the MCU developed with a process in compliance to the functional safety standard?
- How does the MCU handle random failures?
- How does the MCU handle systematic failures?

Because IEC 61508 and ISO 26262 require functional safety to be considered from the very beginning of the product development phase, it is critical to select an MCU that has been designed from the start for functional safety applications. Such MCUs can themselves carry certification, and may be certified to a particular safety integrity level (or "SIL"). A 'certified' MCU means that its development process was reviewed and it is suitable for use in a functional safety system up to the specified SIL.

IEC 61508 provides for MCU certification from a SIL 1 (lowest) to a SIL 3, which is the highest SIL level for MCUs; only the system is capable of being SIL 4. ISO 26262 has a parallel "ASIL" rating, or "Automotive Safety Integrity Level," A through D. ASIL A is the lowest safety integrity level and ASIL D is the highest safety integrity level. Under ISO 26262, MCUs can be certified to all four ASIL levels. The standards require that certified MCUs provide supporting documentation and tools such as the safety manual and failure mode effect and diagnostic analysis (FMEDA) tool to help users understand the MCU's safety mechanisms and to calculate the MCU failure rate.

Examples of 'certified' MCUs are TI's Hercules TMS570 and RM MCUs, which are suitable for use for IEC 61508 up to SIL3 and for ISO 26262 up to ASIL-D, the highest safety integrity levels in the respective standards.

Although there are no requirements in most functional safety standards that end product system developers use a 'certified' functional safety component, such use can help significantly reduce effort and system certification cost. Certified components come with the data and documentation forming the technical functional safety basis needed for the examining agency to accept the component. *In two further sections, the complete article goes to discuss managing random failures; and hazard analysis and risk assessment – click for pdf.*

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Find functional safety in MCU-based designs on EETsearch

OPTIMISING DISPLAY IMAGE QUALITY AND POWER CONSUMPTION BY VARYING FRAME RATE

By Gi Young Lee, Exar

Dynamically changing the refresh rate of a flat panel display can help balance the conflicting demands of image clarity versus power usage. However a special circuit is also needed to provide real-time adjustment of the pixel common voltage as the frequency changes to ensure acceptable flicker-free image quality and to preserve display lifetime.

Flat panel displays based on liquid crystal or organic LED technologies currently use a fixed frame rate between 30 Hz and 240 Hz. If the rate is at the low end, power consumption is reduced, but at a cost of image smearing and a loss of display quality for fast-motion images. For this reason, there has been a trend in high-end televisions to higher frame rates of 240 frames per second (fps), which eliminates any residual images such as multiple images of a golf ball in flight.

However, the drawback of high frame rates is an increase in power consumption, as the display panel has to execute multiple cycles of refreshed image generation within the same time period as for a single refresh cycle at the slower rate. These higher frame rates will have a major impact on run-time on mobile platforms such as a notebook PC.

There is an alternative between these two extremes of low rate/low power and high rate/high power. Future display panels will adopt a technique that adaptively adjusts frame rate based on the contents being displayed and image need. For spreadsheets or word processing, a frame refresh rate below

30 Hz is fast enough, while the same display panel may be set to run at a 240 Hz frame rate when displaying fast-motion game scenes.

However, there are practical problems associated with increasing the frame with the typical liquid crystal or organic display (LCD or OLED) panel, as their optimum electrical operating point may change as the frame rate is varied, due to the physics of their technology and manufacturing issues. These displays use a thin-film transistor (TFT) backplane to control each pixel, turning these TFT devices on and off, Figure 1. The TFT gate voltage is applied to a specific row of a panel, allowing the flow of current from the source voltage for the relevant column, in order to construct the pixel image by adjusting the light-transparency level.

This is done by adjusting the potential across the associated capacitor using an indium tin oxide (ITO) electrode, which is a near-transparent conductive layer of the display. Since these transistor arrays are deposited by thin-film deposition techniques, the quality and consistency of the transistors (which are acting as switches) is far from ideal.

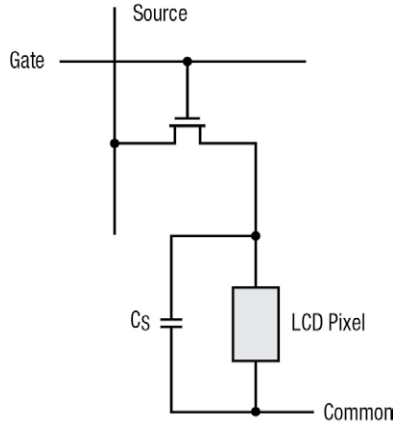


Figure 1. *A simplified schematic of a TFT LCD pixel element*

In typical TFT panels for TVs, where sizes span 30 to 80 inches, the source voltage can range from 0 to 24V. As the panel size grows, the maximum source voltage also must increase as the drive-current requirement increases. The bottom connection of the pixel is usually connected to the backplane; this node voltage is called the common voltage or VCOM

and should be maintained at a single potential across the entire panel area. Further, in order to prolong the life of a panel as well as not have a flicker problem, VCOM is typically established at about the mid-point between zero and the maximum source voltage level, equivalent to about one half of analogue supply, AVDD. (Note that the common voltage VCOM is a true “common” and is not a "ground.")

Little-known TFT characteristic is key

Since the TFT backplane is fabricated by large-area thin-film deposition, the optimal value of the VCOM voltage will differ from panel to panel due to manufacturing variations, even within a single production line. It may also vary within a single panel if the size of the panel is large enough. As a result, the last inspection point of a panel module assembly is to perform a display quality test, which involves factory calibration and adjustment of the optimum VCOM voltage setting for each panel.

With these panels, it is important to manage VCOM to be uniform across the panel as well as over the transient period as the pixel information changes. In most panels, this is done by using between one and 12 channels of operational amplifiers, often called VCOM buffers, linked to the digital/analogue converter (DAC) outputs of digital potentiometers used for storing factory-set voltage levels, Figure 2.

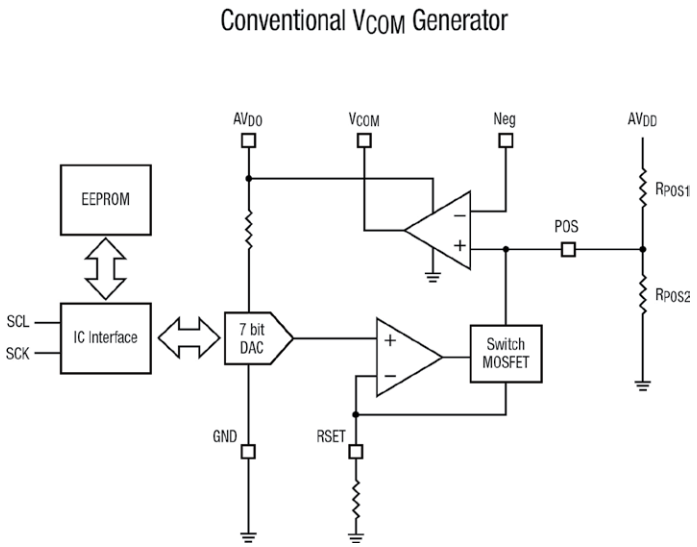


Figure 2. *Typical VCOM generator used today consists of a non-volatile memory, DAC and buffer amplifier*

When the VCOM voltage is perturbed by an image-changing signal, it changes from the set voltage level. The VCOM buffer amplifier will then source or sink an output-node current such that the voltage will return to the set level stored by the digital potentiometer. The amount of energy needed to restore the VCOM output node depends on the degree of offset generated by the transient as well as the supply voltage level, at a given frame rate, which is typically between AVDD and ground. This operation assumes a fixed frame rate.

However, the situation is likely to become more complicated as displays move toward variable frame-rate (refresh rate) operation for many applications. In this scenario, the PC would display images of a spreadsheet or word-processing application at a slow 30 frames/sec, while shifting to a much-higher rate, up to 250 frames/sec, for the fast-moving motion image of a high-end game.

Variable frame rate implementation challenges standard design

The relatively new concept of ‘adaptive sync’ format demands wide-ranging variable frame rates from a stand-alone monitor or laptop display. Varying the frame rate requires real-time adjustment of VCOM in order to avoid any flickering resulting from an initial, non-ideal VCOM setting, as the ideal VCOM level changes with the frame rate.

The article continues, offering an implementation approach for this strategy, click for pdf

DON'T OVER-CONSTRAIN IN FORMAL PROPERTY VERIFICATION (FPV) FLOWS

By Anders Nordstrom, Synopsys

Formal property verification (FPV) is increasingly being used to complement simulation for system-on-chip (SoC) verification. Adding FPV to your verification flow can greatly accelerate verification closure and find tough corner-case bugs, but it is important to understand the differences between the technologies.

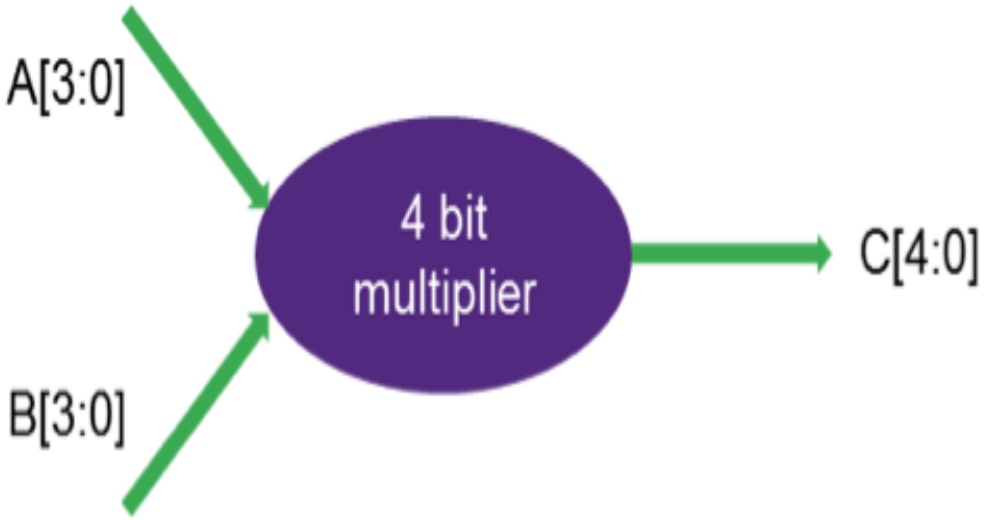
The main difference is that FPV uses properties, i.e., assertions and constraints, instead of a testbench. Assertions are used in simulation as well, but the role of constraints is different. An understanding of constraints is necessary for successful use of FPV.

Constraints

Constraints play a central role in FPV. They define what is legal stimulus to the design under test, i.e., what state space can be reached. Assertions define the desired behaviour of the DUT for the legal stimulus.

Constraints describe how inputs to the DUT are allowed to behave, what values should be taken, and temporal relationships between inputs. Constraints can be thought of as the stimulus in simulation. In constrained random simulation, the constraint solver generates an input vector for the next cycle that satisfies all constraints. It will continue to generate cycle after cycle of stimulus until the end of simulation, or until it reaches a situation where no legal stimulus can be generated.

In contrast, constraints for formal verification can describe, for example, how to legally communicate within a given protocol.



Over and under-constraining

Writing constraints that exactly describe all legal stimuli is difficult and often undesirable. This means that the formal environment is either under- or over-constrained. Under-constrained means that there are fewer constraints than required to exactly model the stimulus. This means that some potentially illegal inputs will be driven to the device under test (DUT). Over-constrained means that there are more constraints than required, and not all legal behaviours will be allowed.

Having a slightly under-constrained environment is usually the best approach. Many designs can handle inputs and behaviours not defined in the specification, and a larger state space in the design will be verified if fewer constraints are used. An under-constrained environment may lead to failing assertions, and if this is the case, additional constraints need to be added. For example, let's say we have a 4-bit multiplier to verify:

The specification says it can multiply positive integers A and B > 0, but the verification engineer assumes A and B >= 0. The constraints and the assertion to check the multiplier is simply:

```
assume property (@posedge clk) A >= 0;
assume property (@posedge clk) B >= 0;
assert property (@posedge clk) C == A * B;
```

If the property is proven in this case – for either or both A and B being zero as well as for positive integers – then obviously it will hold for A and B only being greater than zero. The constraints allowed for additional behaviours, which means the environment is under-constrained. Having fewer constraints usually also improves run time of formal tools. If the properties pass, we don't have to worry about the under-constraining case any more.

Over-constraining the formal environment is a much bigger problem as

... *article continues, click for pdf*

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designideas

- Active load handles high voltages
- Shunt circuit clips large transients or regulates voltage

Active load handles high voltages

By Gheorghe Plasoianu

Bench electronic loads are usually rated for voltages less than 100V, which make it difficult to test high-voltage power supplies. This Design Idea offers an alternative: an inexpensive electronic load rated for 500V or more, depending on the selected components. It is basically a buck converter whose input is the power supply under test. As a load for the output of the converter, a 1000W electric kettle filled with water is used, whose resistance R1 amounts to about 53Ω.

Unlike conventional buck converters, the input current – not the output voltage – is sensed by the error amplifier of the controller. Therefore, it is an average current-mode controller whose outer feedback loop is missing. Specific to this architecture, the inductor acts like a current source feeding the output impedance R1||C2. Thus, we have a single pole system which makes compensation easier. The GBW of U2 must be high enough to avoid adding additional poles in the loop gain. The switching frequency is 50 kHz, so that the power loss of the MOSFET and D1 is low enough to make a heat sink unnecessary.

The voltage drop across the shunt R_{sh} – which is proportional to the current flowing through the power supply – is amplified, inverted, and sent to the feedback input of the regulator.

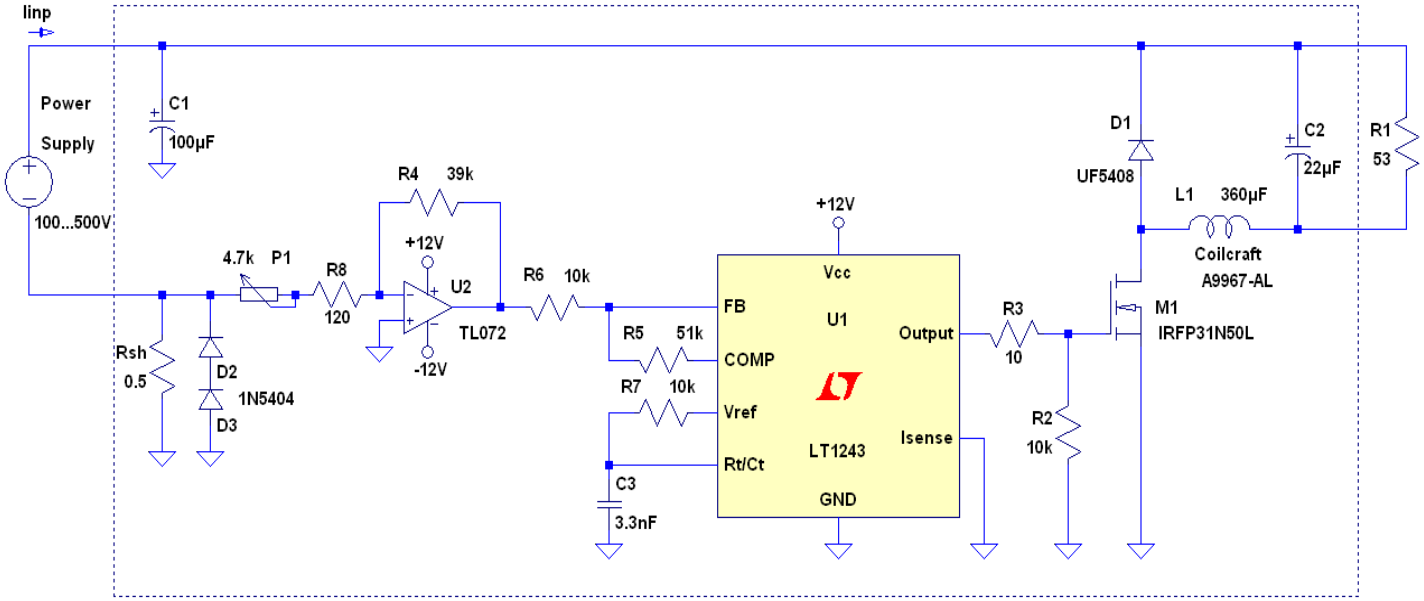


Figure 1. *High-voltage-capable electronic load using LT1243*

The current drawn from the power supply is adjusted with the potentiometer P1.

With the values of the components in the schematic, according to the equation:

$$V_{ref} = -I_{inp} \cdot R_{sh} \cdot R4/(P1+R8)$$

the load current range is: I_{inp} = 15mA…618mA

Diodes D2 and D3 protect the op-amp's input against inrush current drawn by C1 when the power supply is connected.

Reference:

Switching Power Supply Design, Abraham Pressman

Shunt circuit clips large transients or regulates voltage

By Peter Demchenko

The circuit in Figure 1 is a high-power analogue of the popular TL431 programmable shunt regulator. This two-terminal circuit is convenient when the drain of the P-channel FET is grounded, since it needs no isolation from a grounded heatsink.

There is no mirror analogue of the TL431 however, so when you have a positive ground, you need isolation between the drain and the grounded heatsink, degrading cooling performance.

The Design Idea presented in Figure 2 allows the use of a lower-cost N-channel MOSFET on a grounded heatsink. It also tolerates lower values of input voltage than Figure 1.

The circuit can be used as an adjustable clamp capable of high power dissipation, with precise level control and very sharp response. The ballast resistance R_b can be replaced with a fuse if desired. Response time is not as fast as a Transil/Transzorb type of part, but a few microseconds is enough for the most applications. The circuit can also serve as a high-current shunt regulator, though with stability caveats. The circuit is stable with a load capacitance

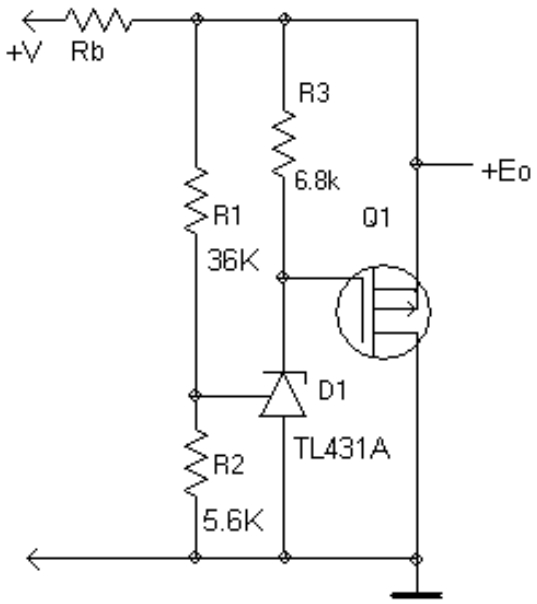


Figure 1. *TL431-based shunt regulator or clipper*

below about 1nF or above about 200 µF. The circuit can be scaled up easily: just select a FET with a suitable drain current. The 75A HUF75652G3 and 85A IRF1010N have been used.

Zener diode D2 can be omitted if:

$$V_{G(max)} > E_O \times R5 / (R4+R5)$$

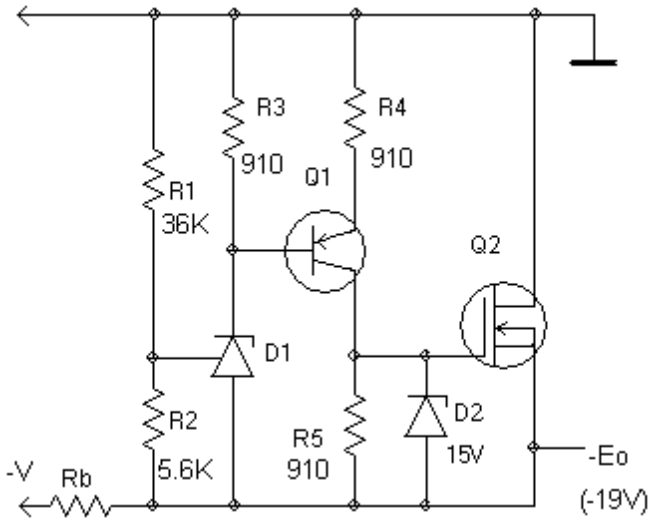


Figure 2. *TL431-based shunt regulator or clipper using N-channel MOSFET*

The clamp voltage is calculated using the same expression as for the TL431:

$E_O = V_{REF}(1 + R1/R2)$ $(V_{REF} = 2.5V)$

Absolute maximum ratings are also the same as for the TL431, except for current of course. The minimum input voltage is about 0.8V higher than for the TL431 alone.

Also see:

High-power shunt regulator uses BJT & reference IC

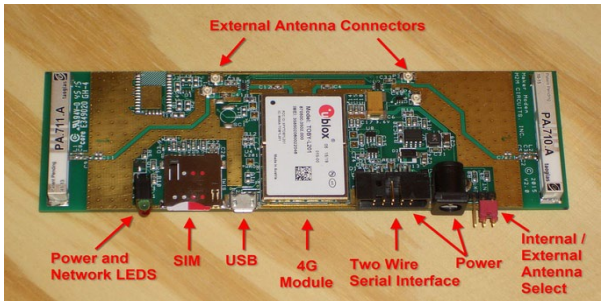
Power Zener using the LM317

productroundup

productroundup

4G LTE M2M modem hosts u-blox module

U-blox' TOBY-L2 LTE module has been embedded in what is claimed as the first 4G LTE Maker Modem by M2M Circuits - now running a campaign on Kickstarter. The 4G modem is designed for the "MakerSpace" enabling direct cellular connection to single-board computers and microcontrollers for M2M applications. In addition to offering high-speed TCP/IP over the LTE network for higher data-rate M2M applications and broader coverage, the Maker Modem is also provisioned for SMS enabling communication by text messages.



Complete article, here

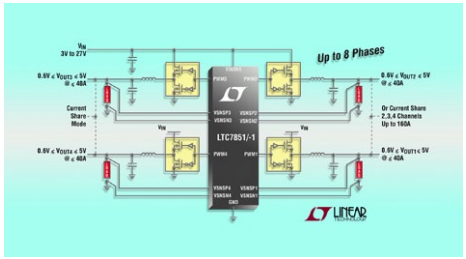
Capacitive multi-touch uses metal mesh – from 3M

Providing, according to makers 3M, easy integration and an "exceptional interactive experience", is a projected-capacitive system incorporating ultrafine Metal Mesh Technology. At three microns wide, the ultrafine mesh conductor allows a more vibrant, high quality optical viewing experience when integrated into a Multi-Touch Display, including curved display panels. Other features include the ability to project through glass up to five millimetres thick, a bezel-free design and support for up to 80 simultaneous touch points; the system supports palm rejection, with a response of under 10 msec.

Complete article, here

4-output multiphase step-down DC/DC: up to 260A

LTC7851/-1 is a quad output multiphase synchronous step-down DC/DC controller with accurate current sharing between phases and differential output voltage sensing. Up to eight phases (with two ICs) can be paralleled and can be clocked out-of-phase to minimise input and output filtering for very high current requirements up to 260A. This controller works in conjunction with external power train devices such as DrMOS and power blocks as well as discrete N-channel MOSFETs and associated gate drivers, enabling flexible design configurations.



Complete article, here

ARM extends Keil MDK MCU tools

MDK Version 5.20 extends the ARM Keil MDK standard software development solution for ARM based microcontrollers, with support for Cortex-A processor-based catalogue devices, connectivity for the Internet of Things (IoT), C language support for C++11/C++14, and the ARMv8-M architecture. Keil MDK Professional Edition Version 5.20 includes DS-MDK: this combines the Eclipse-based DS-5 IDE and Debugger with CMSIS-Pack technology and uses Software Packs to extend device support. Initially the NXP i.MX series is supported; that range offers computing power for application-rich systems with real-time responsiveness as it combines Cortex-A and Cortex-M processor cores. MDK-Professional includes middleware for USB, graphic displays, file system, and networking that is optimised for Cortex-M processors. New is the IPv4/IPv6 networking communication stack that is extended with ARM mbed software, for IoT applications.

Complete article, here

productroundup

MOSFET relays step up current capacity

High current MOSFET relays can support continuous loads of up to 3.3A AC, or 6.6A DC. High current Omron types G3VM-61GR2 and G3VM-61HR1 match the performance of comparable Omron electromechanical relays, and exceed that of competing solid state relay alternatives. Key features are the low on-resistance compared to electromechanical devices and their low susceptibility to external magnetic interference. A key feature is the fast switching time – with a Ton / Toff of 3 msec/0.5 msec for the GR2 and 5 msec/1 msec for the HR1.

Complete article, here

ST claims peak energy efficiency for Cortex-M4 MCUs

STMicroelectronics says it achieves highest-yet microcontroller power savings and performance with its latest STM32L4 series devices. The microcontrollers also introduce peripheral and package configurations that simplify design and increase flexibility. Measured using the EEMBC ULPBench tests for low-power microcontrollers, STM32L4 devices achieve 176.70 ULPMark-CP, without the help of a buck converter that adds external components such as a coil and capacitor. The EEMBC CoreMark score of 273.55 at 80 MHz shows that the STM32L4 series delivers a combination of high peak performance and energy efficiency.

Complete article, here

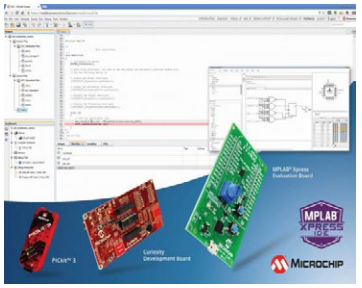
Fast LVDS isolators eliminate de-serialising

Analog Devices has introduced a low-voltage differential signal (LVDS) digital isolator series designed to improve performance, reliability and power consumption in industrial instrumentation and programmable logic controller (PLC) applications that previously required redesign of the interface to support LVDS signal isolation. Incorporating ADI's iCoupler digital isolator technology, the ADN465x series ensures safety and reliability through galvanic isolation in a single package while delivering data throughput rates of 600 Mbps (up to four times faster than competing digital isolators), ultralow jitter at 70 psec, and 4.5-nsec max propagation delay. With ADN465x devices, high-speed serial LVDS signals can now be directly isolated without needing to deserialise as compared to previous custom implementations. Design resources and time are saved by offering an off-the-shelf, high-performance, LVDS-compatible solution.

Complete article, here

Farnell element14 to back Atmel Xplained concept

Farnell element14 and Atmel have launched the SAMA5D2 Xplained Ultra evaluation kit for the fast prototyping and evaluation of Atmel's SMART SAMA5D2 microprocessors. With its secure design architecture, cryptographic acceleration engines, and secure boot loader, the power-efficient embedded MPU is based on the ARM Cortex-A5 processor and features an advanced user interface and connectivity peripherals. Security is provided by cryptographic accelerators, by the ARM TrustZone technology securing access to memories and sensitive peripherals, and by hardware features.

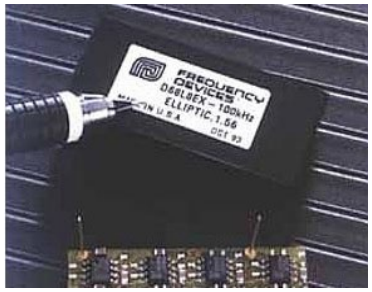


Complete article, here

productroundup

Analogue filters minimise distortion

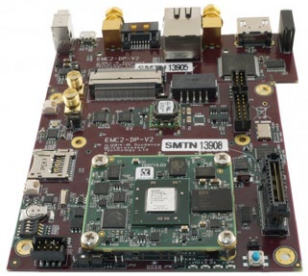
The D68 series of 8-pole analogue filters from Frequency Devices exhibits THD (total harmonic distortion) levels as low as -100 dB with near-theoretical frequency response. Offered in low-pass and high-pass versions with Butterworth, Bessel, elliptic, and constant-delay transfer functions, the D68 series provides linear active filtering in a small 32-pin DIP package. Each model comes factory-tuned to a user-specified corner frequency between 1 Hz and 100 kHz. Units can be combined to create custom band-pass or band-reject filters. The self-contained devices require no external components or adjustments and operate over a wide dynamic input voltage range from noncritical ±5-V to ±18-V power supplies.



Complete article, here

SBC with Xilinx' SDSoC for hardware IP acceleration

"A game-changer for programmable embedded systems," - Sundance's EMC2-Z7030 is a stackable SBC with PC/104 One-Bank interface and VITA57.1 FMC, controlled by a Zynq SoC and fully supported by the latest Xilinx SDSoC development environment, that supports migration of performance-critical algorithms and IP into programmable hardware. Sundance's EMC2 range is a family of industrial-grade and deployment-ready SBC's that feature a Xilinx Zynq SoC with integrated dual-core ARM-A9 CPUs coupled to 1 GB of DDR3 memory, four-lanes of PCI-Express and re-programmable logic with Kintex-7 FPGA technology.



Complete article, here

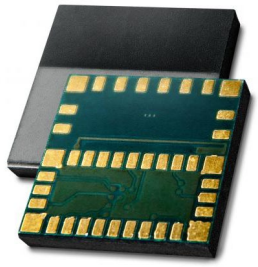
Renesas develops Synergy platform for IoT designs

Expanding its Synergy platform, that is intended to allow system designers to spend as much time as possible on end-applications, and to provide a higher proportion of design 'infrastructure' elements ready-made, Renesas has added the S124 Group of Synergy Microcontrollers (MCUs) with ultra-low power operating characteristics and precise analogue signal acquisition/generation capabilities, configured for sensor applications. The Synergy Software Package (SSP) and the e² studio Integrated Solution Development Environment (ISDE) tool incorporate further enhancements that address the entire Synergy Platform adding new capabilities for networking, industrial automation, power management and automated configuration. Synergy MCUs in the S124 Group are based on Renesas' ultra-low power technology consuming 70.3 µA per MHz.

Complete article, here

Full Bluetooth LE node in 8x8x1mm

Building on its ISP130301 integrated MCU Bluetooth Smart Module, Insight SIP is releasing the ISP1302 as a low-cost option. The 8 x 8 x 1 mm device integrates the nRF51822 chip from Nordic Semiconductor (running Bluetooth 4.1) - offering a 32 bits ARM Cortex CPU, 128 kB flash memory, analogue and digital peripherals SPI, I²C and GPIO. Combined with its integrated 16 MHz crystal, RF antenna and matching circuit, this module forms a standalone Bluetooth Low Energy node. Power consumption is typically 10.5 mA for transmission, 12.6 mA for reception, 2.3 µA for standby mode and 0.5 µA for deep sleep. Transmission output power reaches +4 dBm and reception sensitivity -93 dBm.



Complete article, here

productroundup

Auto power FET with 1.35mΩ on-resistance

This AEC-Q101 qualified 40V DPAK+ MOSFET claims lowest on resistance of just 1.35mΩ at 10V drive. In Toshiba's UMOS9 MOSFET series, it is packaged in DPAK+. Applications include automotive motor control applications such as water pumps, fuel pumps, oil pumps, fans, EPS; and DC/DC converters. This MOSFET achieves RDS(ON) = max1.35 mΩ at VGS=10V – the lowest RDS(ON) of any MOSFET currently available. It does so by combining UMOS9 trench technology that minimises RDS(ON) x A, with the DPAK+ package that reduces package resistance compared to conventional DPAK packaging.

Complete article, here

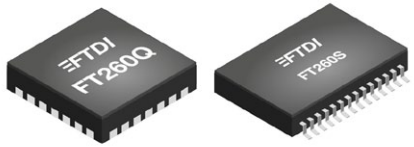
High-efficiency 15-W wireless power transmitter/receiver

Supporting the Wireless Power Consortium's Qi Standard, these chips enable wireless charging in new categories of consumer products and infrastructure, according to makers IDT. The devices comprise a complete high-efficiency package up to 15W output power. They deliver power conversion efficiency of over 86% from transmitter input to receiver output. The P9240A transmitter is suitable for standalone transmitter pads and embedded furniture, as well as infrastructure applications in airports, hotels and cafes. The companion P9220 receiver is designed for products that require high current charging such as tablets and phablets.

Complete article, here

Single-chip USB-to-I²C & USB-to-UART

FTDI Chip has advanced its approach that makes USB technology as straightforward to use as possible. The FT260 is a human interface device (HID) class interface controller IC. It can provide USB 2.0 Full Speed (12Mbps) connectivity to a broad range of application scenarios. Uses include connection of touchscreens, computer peripherals and IoT sensing apparatus, as well as USB interfacing of microcontroller or programmable logic centric system designs, plus industrial automation equipment and USB instrumentation.



FTDI Chip | BRIDGING TECHNOLOGIES

Complete article, here

IoT sensor-to-cloud from Analog hosts personal-measurement apps

Analog Devices and Consumer Physics (Tel Aviv, Israel) have collaborated on an IoT Platform that enables material analysis of food, drugs and more, for quality, content and composition. The sensor-to-cloud personal and industrial IoT platform analyses liquids and solids, including food, plants, drugs, chemicals, the human body, and a variety of other materials. The two companies plan to embed CP's SCiO technology for material sensing into smartphones, wearables, industrial, and medical applications. The co-developed sensor-to-cloud platform will enable users to detect substances quickly and reliably, control quality, and measure a wide range of characteristics such as calories, fat, sugars, and proteins; sugar content (as Brix the sugar concentration of a liquid), in fruits and vegetables; alcohol content in beverages; and chemical composition of fuel and oil. SCiO's underlying science is Near-Infra-Red (NIR) Spectroscopy.

Complete article, here

CONNECTED DEVICES – SECURITY STARTS WITH SOFTWARE DESIGN

BY BY MARK WARREN, PERFORCE SOFTWARE

Hackers love a challenge and the evolution of connected devices presents them with a whole new world to exploit. There have been tales of all kinds of products being infiltrated, from the remote takeover of a Jeep Cherokee by Charlie Miller and Chris Valasek through to anecdotes of life-saving medical equipment being compromised in a hospital.

Of course, security vulnerabilities can creep in at all kinds of entry points during a product's lifetime, but it is essential to get the basics right in the first place, back when the product is being developed. And since software is driving much of the innovation around connected devices, then it is vital to put the spotlight on software development processes, whether we are talking about embedded software or communications software.

This is new territory for a lot of today's electronics engineers. Security is not something they have generally had to worry about (apart from making sure the lab was locked at night). Suddenly, they are being tasked with creating products that are not only fit for purpose, but that are equipped to withstand the efforts of persistent hackers (who let's face it, are not people who tend to give up easily). It matters, because the consequences are pretty scary: someone emptying a million bank accounts is bad enough, someone disabling a vehicle or medical equipment could have truly devastating consequences.

The scale is pretty daunting too: a connected device might involve multiple electronic control units (ECUs) and sensors. Computer code may need regular updates, perhaps far more than previously, including over-the-air releases. Separating out systems is an obvious step that many designers have already taken, so that 'mission critical' elements are separate from more mundane elements. However, in today's connected world, it is impossible to disregard the volume of external communications that have to take place, such as remote diagnostics. The sheer volume of vulnerable entry points is huge.

So what is the answer? There is a lot that can be done to ensure better protection, including reinforcing some existing software design 'best practice' steps, such as having greater visibility across the entire software development process, across all contributors. Not only does this engender a more collaborative approach (important to most successful software development projects), it ensures that the history of that software's development is available for scrutiny, both now and in the future.

Tighten up on processes around coding languages

While I'm not suggesting immediately moving away from popular coding languages such as C and C++ - into which many firms have heavily invested – the fact is that they can pave the way for security attacks, for example through format string attacks, buffer overflows, dangling pointers and privilege escalation bugs. In the

automotive world, the MISRA coding standards have done a lot to prevent vulnerable code being created in the first place. Use of static analysis tools can help by scanning source code (version control) repositories to pick up non-compliant code, or to identify flaws or even potential vulnerabilities. Other types of tool can be used to catch policy violations, flow analysis, code reviews and run-time errors, memory leaks and buffer overflows that occurred during the build and test stages of the project.

Taking a more holistic view of software and hardware design makes it easier to have a single approach to handling security across the device design and development process. Related assets, for instance, requirements, designs, test scripts – and the code associated with software should be considered as a whole and modern version management systems make it possible to manage all such assets in a single repository. The good news about this approach is that it becomes much easier to avoid gaps or misunderstanding across different teams, or team members responsible for different tasks.

Integration is everything – software development projects typically involve multiple contributors, both internally and by external third-parties. It's not unusual for an electronics design project to have dozens, if not hundreds, of suppliers involved. These third-parties may be collaborators, but they are unlikely to have any real visibility into the overall hardware and software development process. The problem with that is the buck stops with the manufacturer, so if something goes wrong, then they really do need to have detailed information about how every component in a connected device was developed (by whom, when, where and how).

Ultimately, we may see a more open, standardised architecture across all connected devices (there is already movement in the connected car industry, for instance), but in the meantime, many organisations are using their version control tools to create a more collaborative and transparent environment across contributors both internally and externally, thus creating an 'audit trail' of the whole development process. It is usually pretty important that the version control system is technology-agnostic, as realistically, there are going to be multiple platforms and tools involved.

Other attributes to look for include in-built security and the ability to scale to manage large volumes of assets, not just code but other content, for instance CAD drawings or prototype designs.

Given the dependency of connected devices upon software, security vulnerabilities are going to continue to become an important focus and while cast iron security is probably an impossible goal, there is much that can be done during the development process itself to help prevent future problems.

About the Author

Mark Warren is product marketing director at Perforce Software, providers of scalable source code management (SCM) and collaboration tools that enables global teams to collaborate on any type or size of file. He has more than two decades of experience in the software industry with roles as a provider and consumer of advanced development tools.
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